Illuminance sensor, part 1: design

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1 Introduction

This is a report on an assignment for a course in process measurement technology. The task is to design, simulate, construct, test and calibrate an analog illuminance sensor based on an LDR.

This is the first part which only covers design and simulations as well as all information needed for construction.

The report is a bit of a mess, but all the important stuff that has been thought about can be found somewhere.

Contents

1.1 Required specifications

Parameter	min	max	unit
Sensor component			PGM5526
Illuminance range	0	1 000	Lux
Illuminance range	0	100 000	Lux
Ambient temperature	0	70	°C
Supply voltage (V_S)	19	29	V (single ended)
Analog voltage output	0	10	V
Analog current output	4	20	mA
Load resistance	0	500	Ω
Number of digital outputs	1		

There also needs to be a way to calibrate the sensor.

1.2 Specifications

The sensor meets the listed required specifications.

Miscellaneous features:

- The `range_select` input is used for switching between 0 to 1000 Lux (logic low) and 0 to 100 000 Lux (logic high). It is desgined for current sourcing 24 V logic.
- The voltage output is limited to 10 V max to stay within specifications (if properly calibrated). If the illuminance exceeds the selected range, the digital output `over_range` will go high. (The current output is dervied from the voltage output.)
- The comparator output $\overline{\texttt{digital}}$ is high when it's darker than a threshold set with P8. The comparator also has user settable hysteresis with P9. **This signal should be renamed to `dark` as that name would make more sense**.
- The LDR is planned to be outside of the enclosure to make the actual sensing part less bulky.
- The digital outputs have been designed to be able to directly drive a small load, with the exception that it has no short circuit tolerance.

Additional specifications.

Parameter	**min**	**max**	**unit**	**comments**
Power draw (current)		340	mA	see section 3.3
Supported LDR R_{10}	8	20	kΩ	
Supported LDR γ	0.5	1.0	1	
Light range with `range_select` low	0	1 000	Lux	
Light range with `range_select` high	0	100 000	Lux	
`range_select` low voltage	-16	0	V	see section 2.4.2 and 3.7
`range_select` high voltage	18.2	$V_S + 16$	V	
`analog_voltage`	0	10	V	
`analog_voltage` load current	0	20	mA	source only
`analog_voltage` short circuit dur.		brief	s	see section 2.3.1
Linearity	$U \propto \sqrt{E}$	$U \propto E$	-	$U \propto E^{\gamma}$, E is illuminance
`analog_current`	4	20	mA	
`analog_current` load voltage	0	10	V	normal operation
`analog_current` open circuit vol.	10	V_S	V	fault condition
`analog_current` open circuit dur.		∞	s	protected
Comparator trigger level	0	10	V	
Comparator hysteresis resistor	47	1047	kΩ	trigger pot is 10kΩ
Digital outputs, high, voltage	$V_S - 1$	V_S	V	
Digital outputs, high, load current	>0	100	mA	
Digital outputs, low, max sink		0	mA	source only
Digital outputs, low, *unloaded* voltage	0	V_S	V	high impedance
Digital outputs, high, short circuit dur.		0	s	no protection

Further information for usage, including transfer functions, is in section 6 - Usage

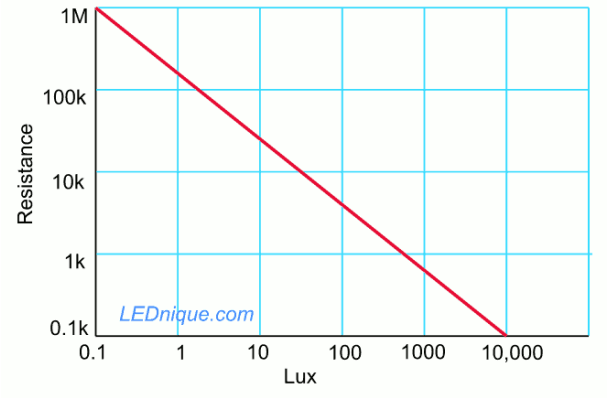
1.3 Planning

1. Sketching and simulating in LTspice
2. Starting documentation
3. Make PCB layout in Eagle and also get a nicer looking schematic
4. Mechanical design
5. Bodge in mounting holes in PCB layout

2 Theory of operation and schematic

2.1 LDR characteristics

The conductance of the LDR is (non-linearly) proportional to the illuminance:



Example graph from LEDnique

The resistance R of an LDR (light dependent resistor) is

$$R = R_{10} \cdot \left(\frac{10\ Lux}{E} \right)^{\gamma}$$

where E is the current illuminance (in Lux), R_{10} is the resistance at 10 Lux, and γ is the gamma characteristic.
Sources: LEDnique, Electronics StackExchange

The PGM5526 datasheet specifies:

parameter	**min**	**max**
R_{10}	8 $k\Omega$	20 $k\Omega$
γ	0.6	(not specified)
Dark resistance	1 $M\Omega$	
Max power	100 mW	
Rise time		20 ms
Decay time		30 ms

Elsewhere the datasheet specifies a tolerance of 0.1 for γ, so maybe it's actually a nominal value. But we can assume 0.5 is the minimum.

Let's assume γ is either less than/equal to one or more than/equal to one. And because γ_{min} is less than one, I will assume that $\gamma_{max} = 1$ is a reasonable value.

The operating range of the device will be 0 to 1000 and 0 to 100 000 Lux, which will cover a wide range of resistance.

1 Lux, 1000 and 100 000 Lux resistances at various R_{10} and γ:

$\boldsymbol{\gamma}$	0.5			0.6			0.7			1.0		
$\boldsymbol{E}$	1	1 k	100k	1	1 k	100k	1	1 k	100k	1	1 k	100k
$\boldsymbol{R_{10}}$												
8 k	25.3 k	800	80	31.8 k	505	31.8	40.1 k	318	12.7	80 k	80	0.8
12 k	37.9 k	1.2 k	120	47.8 k	757	47.8	60.1 k	478	19.1	120 k	120	1.2
16 k	50.6 k	1.6 k	160	63.7 k	1.01 k	63.7	80.2 k	637	25.4	160 k	160	1.6
20 k	63.2 k	2.0 k	200	79.6 k	1.26 k	79.6	100 k	796	31.7	200 k	200	2.0

To get the best linearity, the circuit should measure the conductance of the LDR. Full scale conductance for the 1 000 Lux range can be anywhere between $\frac{1}{2\ k\Omega} = 0.5\ mS$ and $\frac{1}{80\ \Omega} = 12.5\ mS$, and for the 100 000 Lux range it can be anywhere between $\frac{1}{200\ \Omega} = 5\ mS$ and $\frac{1}{0.8\ \Omega} = 1250\ mS$.

2.2 Complete schematic (LTspice)

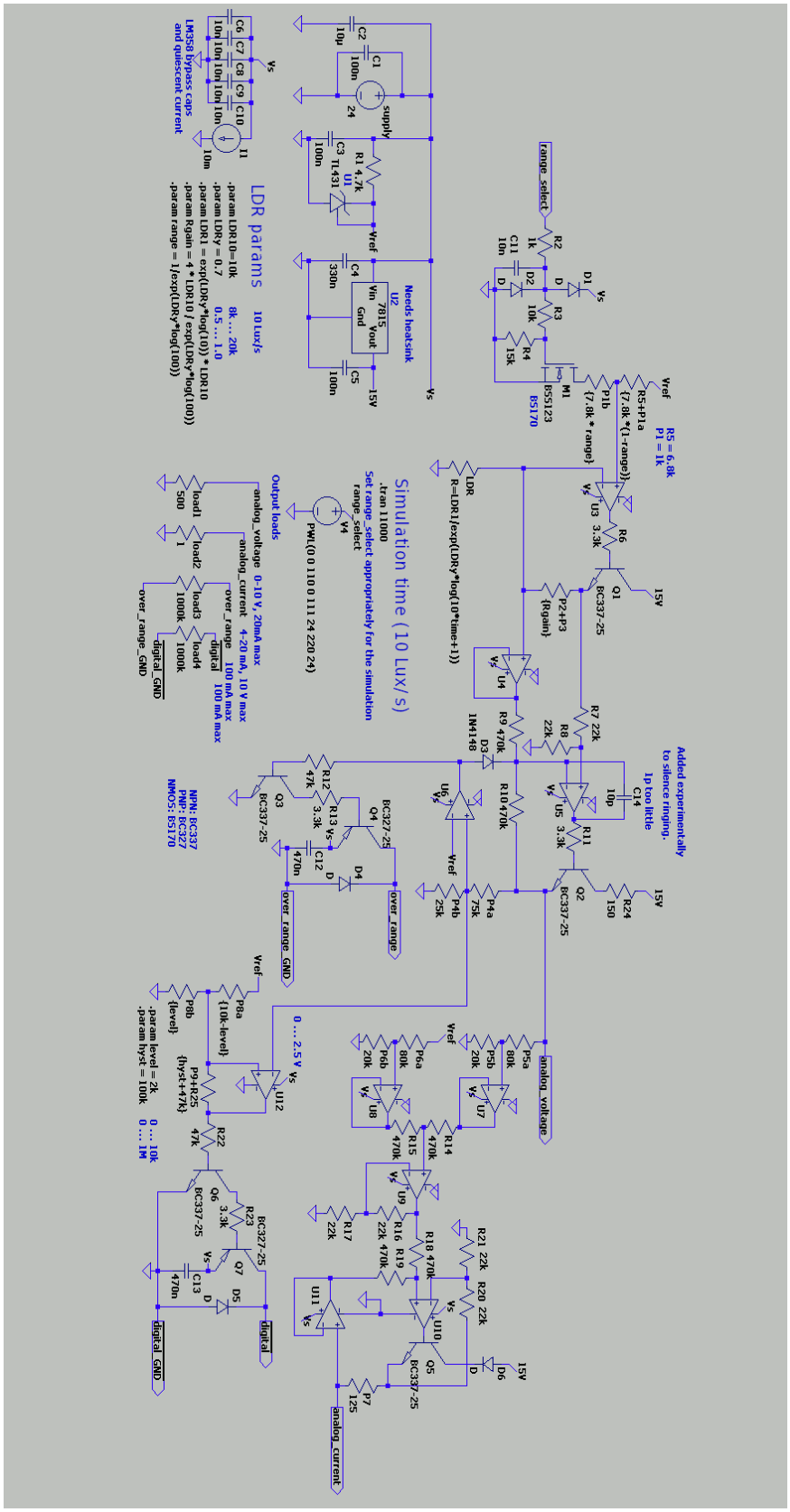
On the side is the complete schematics (made in LTspice).

Each part will be explained in detail in later sections.

Notes:

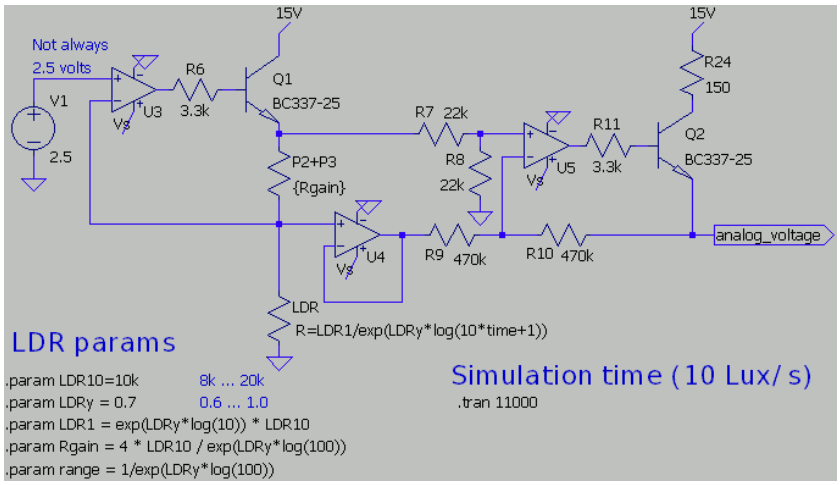
- The BSS123 is actually supposed to be a BS170, but the exact component isn't important.
- *Update:* C14 should be 100 pF.

The LTspice circuit can be downloaded from Gitlab. Note that the `7815.*` and `TL431.*` files are required.



2.3 Partial schematics

2.3.1 Conductance to voltage conversion



U3 with the help of Q1 will maintain a contant voltage

$$\left(\frac{1}{range}\right)^{\gamma} \cdot V_{ref}$$

(where *range* is 1 or 100 and V_{ref} is 2.5 volts) over the LDR. The current is sensed with the combination of P2 and P3, and then sent off to a unity gain differential amplifier (U5) with the sensitive low side through a buffer (U4).

The full scale voltage across P2 + P3 should be 10 volts which is 4 times the reference voltage used. Assuming range is 1 (meaning 1 000 Lux), the correct resistance (R_{gain}) is:

$$R_{1000} = \frac{R_{10}}{100^{\gamma}}$$
$$R_{gain} = \frac{10\ V}{V_{ref}} \cdot R_{1000}$$

The actual value varies between

$$R_{gain,min} = 4 \cdot \frac{8\ k\Omega}{100^{1.0}} = 320\ \Omega$$
$$R_{gain,max} = 4 \cdot \frac{20\ k\Omega}{100^{0.5}} = 8000\ \Omega$$

The 15 V rail exists for these two transistors as well as the current output to limit the amount of power dissipated in the transistors.

The 15 V rail limits the current through the LDR to 1.5 times full scale current:

$$I_{LDR,full} = \frac{V_{ref}}{R_{1000,min}} = \frac{2.5\ V}{80\ \Omega} = 32\ mA$$
$$I_{LDR,max} = 1.5 \cdot I_{LDR,full} = 47\ mA$$

($I_{LDR,full}$ will also be used in some later calculations.)

The power dissipation in P2 + P3 can be as high as:

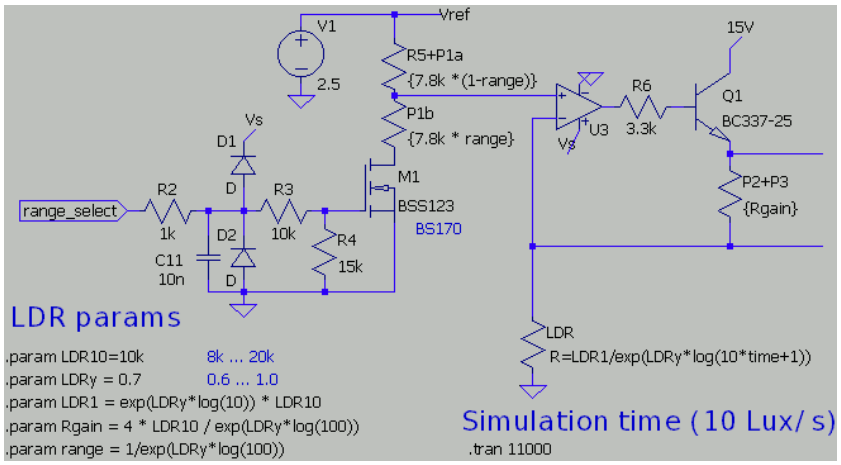
$$P = I_{LDR,max} \cdot 15\ V = 0.7\ W$$

R6 prevents the op-amp from forcing any significant current through Q1 in the even of more than 1.5 times the max illuminance.

R11 protects U5 from a shorted output signal. R24 offers limited protection for Q2 in the event of a short circuit.

R9 and R10 need to be quite large as the voltage over LDR will be very low on the 100 000 Lux scale and the LM358 doesn't have a very good sinking capability at low output voltages.

2.3.2 `range_select`



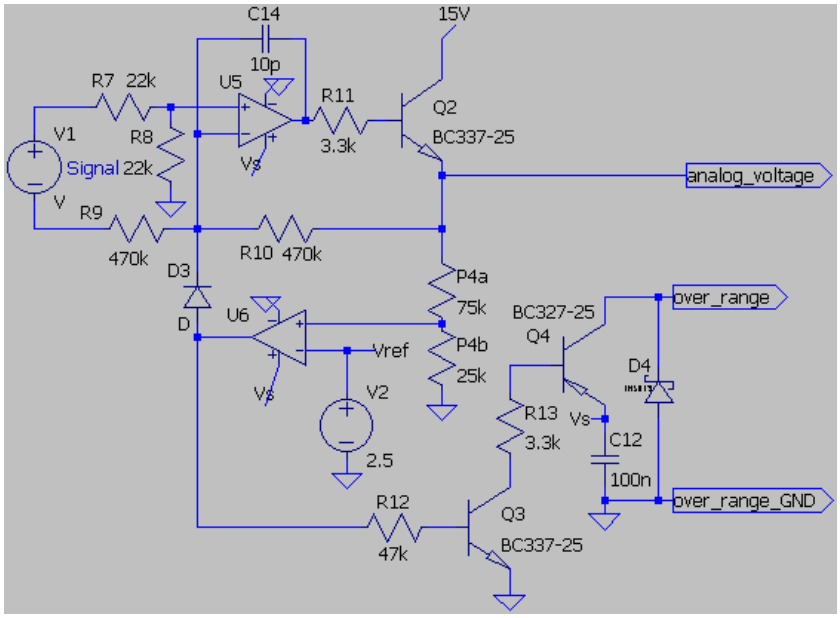
In order to accomodate two different ranges (1 000 Lux and 100 000 Lux) the voltage across the LDR can be reduced by a constant factor. The full scale current will remain the same.

The constant factor is $\left(\frac{1}{100}\right)^{\gamma}$ and is set by a voltage divider consisting of R5 (6.8 kΩ) on the high side and P1 (1 kΩ) with the output at P1's wiper. As γ is known to be between 0.5 and 1.0, the constant factor can only be between 1% and 10% hence R5 is used to eliminate some of the useless range.

When the 24 V digital input `range_select` is high it enables a MOSFET (M1) and hooks the low side of the voltage divider to ground. And when it's low, the divider is left floating for the normal voltage for the 1 000 Lux range.

R2, R3 and R4 reduce the signal voltage to something that can be handled by the MOSFET. R4 also serves as a pull down. R2, C11, D1 and D2 offer ESD protection. C11 also shunts any noise to ground.

2.3.3 Voltage limiter



The output is guaranteed to be from 0 to 10 volts. It can't be less than zero as there it would require the LDR to have negative resistance and also because there is no negative rail. Nothing however prevents it from exceeding 10 volts and it could approach reach 15 volts in sufficiently bright conditions.

The comparator U6 (actually just an LM358 op-amp) will sense if the output starts exceeding 10 V and force the inverting input of U5 high through the diode D3. P4 is used to reduce the signal to a quarter as there is no 10 V reference to use.

P4 must not be too large due to the positive feedback loop!

$$\frac{P4}{P4 + R10} \cdot V_{Supply,max} < 10\ V$$

Other things preventing U6 from causing a latch up:

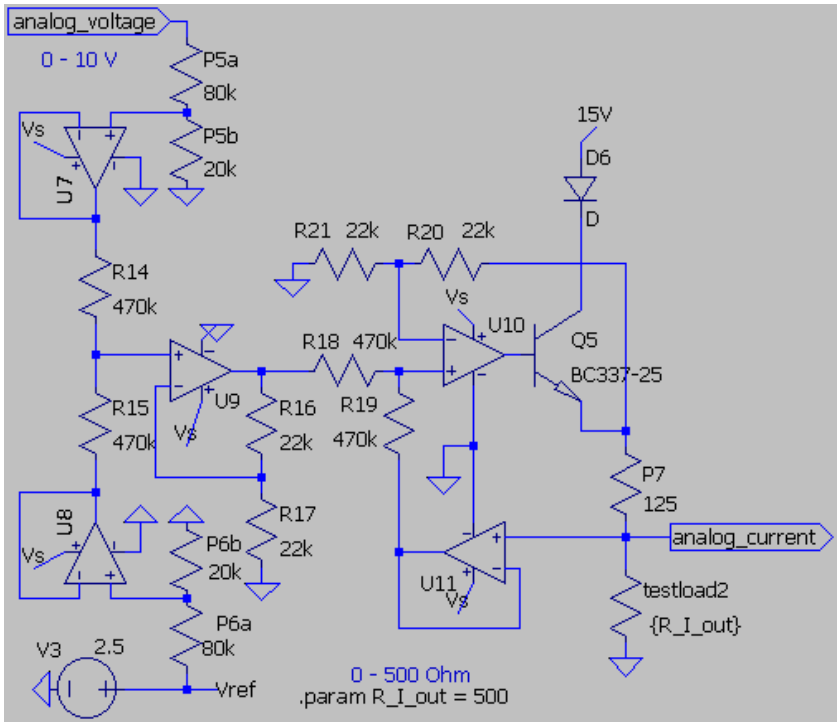
- U6 operates with negative feedback to keep the output at 10 V; the output will not go high enough to cause a lock-up.
- The load is in parallel with P4 and there is a dropout voltage in the op-amp.
- Even without this divider keeping positive feedback through D3 below 10 V, U5 can pull it down through zener breakdown in Q2.

The output from U6 also goes to R12, Q3, R13 and Q4 to form a 24 V PNP open-collector digital output (100 mA), with C12 as a bypass and optionally D4 for protection against inductive loads.

During simulation extreme ringing was noticed when the input rapidly fell from 11 volts to below 1.2. Slowing down U5 with C14 fixed the problem. 1 pF was not sufficient but 10 pF is in the simulation. The time constant of C14 and R9 should be kept a magnitude or more lower than the LDR's response time to avoid any adverse effects.

Update: C14 is 100pF in the final circuit

2.3.4 Voltage to current conversion



The voltage input goes from 0 volts to $4 \cdot V_{ref} = 10\ V$ and the current output goes from $\frac{1}{5} \cdot 20\ mA = 4\ mA$ to $\frac{5}{5} \cdot 20\ mA = 20\ mA$, ie. the output is $\frac{1}{5}$ bias and $\frac{4}{5}$ actual signal.

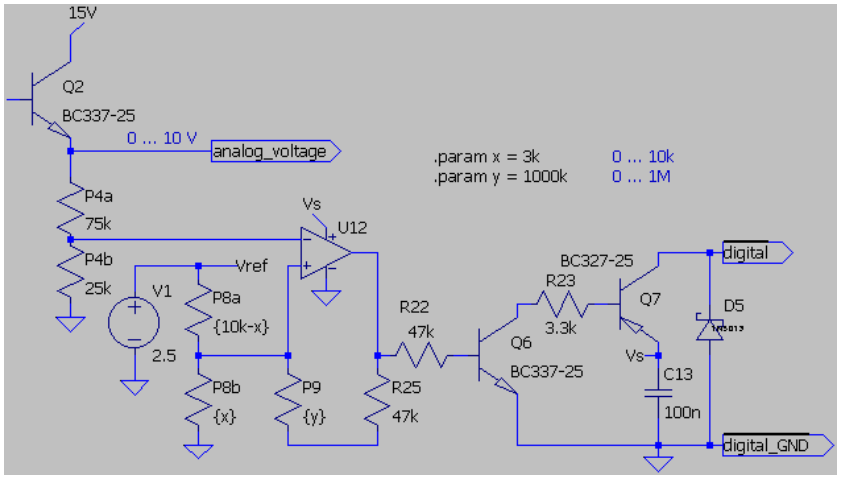
R18 to R21, P7, U10 and U11 and Q5 form a known good transconductance amplifier (*1) with a gain of $\frac{20\ mA}{2.5\ V}$ set by P7 at 125 Ω and support a maximum output voltage of 10 V. Full range input is $V_{ref} = 2.5\ V$

To get the right output from the transconductance amplifier it needs to be fed with $\frac{1}{5} \cdot analog\_voltage + \frac{1}{5} \cdot V_{ref}$. P5 and P6 reduce both the signal and V_{ref} to a fifth and is then buffered by U7 and U8 before fed into an adder consisting of R14 to R17 and U9.

D6 prevents U10 to back-feed the 15 V rail through the collector-base junction of Q5 if the output is open circuit.

*) Transconductance amplifier is taken from a previous assignement. *Update:* The circuit is better explained in part two.

2.3.5 Comparator



P4 is reused to get $\frac{1}{4}$ of the voltage to compare against. P9 should be (user) adjustable as well to allow changing the amount of hysteresis. P8 sets the trigger level. When the analog output is below the trigger level the digital output is high, and low (high impedance) when it's above.

R25 prevents short circuit if both P8 and P9 is set to max. It could be as low as 10 kΩ for this purpose. It also limits how extreme the hysteresis can be and 47 kΩ seemed like a nice value for that purpose.

2.4 Component selections

Resistors are limited to E6 values and capacitors to E3. Resistors are assumed to be of 5% tolerance and 250 mW maximum power dissipation.

2.4.1 Op-amps

The pretty generic LM358 or functionally equivalent LM324 should suffice. Three of the op-amps will sink current all the way down to ground, but can be managed by using very large resistors. The input bias current is approximately three order of magnitude smaller than the maximum sink current (at 0V) and can therefore be ignored.

Maximum output voltage is at least $V_s - 4\ V$, meaning that they can deliver up to 15 V at minimum supply voltage.
Maximum current sink at very low voltage (200 mV) is at least 12 μA.

TI's datasheet for the LM358 recommends a 10 nF bypass capacitor (C6-C10) per chip.

2.4.2 `range_select`

M1 is a BS170 or any other normal N-channel MOSFET in a TO-92 with a DGS pinout. $R_{DS(on)}$ is at most 5Ω.

R5 (6.8k) + P1 (1k) forms a voltage divider with R5 to limit the amount of useless range. The useful range is 1% to 10% (explained in the previous chapter) and R5 sets the upper limit to somewhere between $\frac{0+90\%\cdot 1000}{0+90\%\cdot 1000+105\%\cdot 6800+10} = 11.1\%$ and $\frac{5+110\%\cdot 1000}{5+110\%\cdot 1000+95\%\cdot 6800} = 14.6\%$.

The lower limit is determined by the $R_{DS(on)}$ of the MOSFET and resistance of the wiring. The resistance of the wiring on the transistor side of the potentiometer should be well below one Ohm, or there are bigger problems. The lower limit is at most $\frac{5+1}{5+1+90\%\cdot 1000+95\%\cdot 6800} = 0.082\%$.

The BS170 has a drain cutoff current up to 0.5 μA which is a lot less than 2.5 $V/7.8\ k\Omega = 320\ \mu A$.

P1 is later chosen as a carbon trimmer potentiometer. To minimize thermal drift, R5 should preferrably be a carbon film resistor to match the temperature coefficient.

R2, C11, D1 and D2 offer ESD protection for the MOSFET. C11 should be placed as close to the input as possible. The RC filter will allow basic diodes like 1N4148s or 1N4001s to be used.

R2, R3 and R4 form a voltage divider to take a 19 to 29 volt input signal and reduce it to something suitable for a 10 V ($V_{GS(on)}$) to 20 V $V_{GS(max)}$ MOSFET. R2 and the diodes form a voltage clamp that enforces the voltage across R3 and R4 to stay between -0.7 and 29.7 volts.

1, 10 and 15 kilo ohms are appropriate values for this MOSFET or any similar.

$$R2 = 1\ k\Omega, R3 = 10\ k\Omega, R4 = 15\ k\Omega$$
$$V_{max} = 30\ V \cdot \frac{105\% \cdot R4}{95\% \cdot R3 + 105\% \cdot R4} = 18.72\ V$$
$$V_{min} = 19\ V \cdot \frac{95\% \cdot R4}{105\%(R2 + R3) + 95\% \cdot R4} = 10.49\ V$$

Bug: $V_{GS(th)}$ for the BS170 is specified at $I_D = 1\ mA$. The current through the divider when the transistor is fully on is only 320 μA - while it is high enough to not make the up to 0.5 μA drain cut-off current a concern and low enough to not make the 5 Ω $R_{DS(on}$ another - it is well below the threshold drain current.

The circuit should be fixed to drive the FET hard. But in the current form the issue can be mitigated by specifying $V_{low,max} = 0\ V$.

The resistance values above give the following logic level voltage ranges:

$$V_{GS(on)} = 10\ V, \quad V_{GS(th,min)} = 0.8\ V$$
$$Rn_{min} = 95\%Rn, \quad Rn_{max} = 105\%Rn$$
$$P_{R1,max} = 250\ mW$$
$$V_{high,max} = V_S + \sqrt{P_{R1,max} \cdot R1_{min}} + 0.6\ V = V_S + 16\ V$$
$$V_{high,min} = \frac{R2_{max} + R3_{max} + R4_{min}}{R4_{min}} \cdot V_{GS(on)} = 18.2\ V$$
$$V_{low,th} = \frac{R2_{min} + R3_{min} + R4_{max}}{R4_{max}} \cdot V_{GS(th,min)} = 1.3\ V$$
$$V_{low,max} = 0\ V$$
$$V_{low,min} = -\sqrt{P_{R1,max} \cdot R1_{min}} - 0.6\ V = -16\ V$$

$V_{low,th}$ is the lowest voltage that could get the gate of the FET to its threshold voltage at which it may have an effective resistance in the proximity of $0.8\ V/1\ mA = 800\ \Omega$.

C11 also serves to filter noise. With a capacitance much higher than in the MOSFET, high frequency noise will be shunted to ground.

C11 must not be too large. The LDR has a rise time of 20 ms and `range_select` should be faster than that. The time constant should be kept at least an order of magnitude lower than 20 ms.

$$
\begin{aligned}
&10\tau < 20\ ms \\
&\tau = (R3 + R4) \cdot C11 \\
&C11 < \frac{2\ ms}{15\ k\Omega} \\
&C11 < 133\ nF
\end{aligned}
$$

2.4.3 Bipolar junction transistors and their current limiting resistors

Q1 to Q7 are assumed to have an $h_{FE} \geq 100$. BC337 for NPNs and BC327 for PNPs or any other TO-92 with a CBE pinout, $h_{FE} \geq 100$ and a max power dissipation at 70 °C of at least 400 mW.

$$
\begin{aligned}
&V_{opamp} = V_{S,min} - 4\ V = 15\ V \\
&h_{FE} = 100
\end{aligned}
$$

2.4.3.1 LDR: Q1, R6

R6 limits the current from U3 to prevent it from putting much more than 15 V on P2 + P3.

$$
\begin{aligned}
&V_{e,max} = 12.5\ V \\
&I_{e,max} = I_{LDR,full} = 32\ mA \\
&R6_{max} = h_{FE} \cdot \frac{V_{opamp} - V_{e,max} - 0.7\ V}{I_{e,max}} = 100 \cdot \frac{15\ V - 12.5\ V - 0.7\ V}{32\ mA} = 5.6\ k\Omega
\end{aligned}
$$

The chosen 3.3 kΩ limits the current from U3 during LDR short / over illumination to less than $(29\ V - 0.6\ V)/(3.3\ k\Omega + 320\ \Omega) = 7.9\ mA$

The maximum (LDR shorted and P2+P3 at 320Ω, the minimum) power dissipation in Q1 is:

$$
\frac{(15.75\ V/2)^2}{320\ \Omega} + 7.9\ mA \cdot 0.7\ V = 200\ mW
$$

2.4.3.2 `analog_voltage`: Q2, R11, R24

R11 limits the base current to Q2 / current from U5.

$$
\begin{aligned}
&V_{e,max} = 10\ V \\
&I_{e,max} = 20\ mA \\
&R11_{max} = h_{FE} \cdot \frac{V_{opamp} - V_{e,max} - 0.7\ V}{I_{e,max}} = 100 \cdot \frac{15\ V - 10\ V - 0.7\ V}{20\ mA} = 21.5\ k\Omega
\end{aligned}
$$

The chosen 3.3 kΩ limits the current from U5 during output short circuit to:

$$(29\ V - 0.6\ V)/3.3\ k\Omega = 8.7\ mA$$

R24 limits the power dissipation in Q2 during output short circuit.

$$
\begin{aligned}
&V_{e,max} = 10\ V \\
&I_{e,max} = 20\ mA \\
&V_{15V,min} = 14.25\ V \\
&V_{ce,sat} = 0.5\ V \\
&R24_{max} = \frac{V_{15V,min} - V_{ce,sat} - V_{e,max}}{I_{e,max}} = 187.5\ \Omega
\end{aligned}
$$

R24 is 150 ohms. The maximum power in Q2 is:

$$
\begin{aligned}
&V_{15V,max} = 15.75\ V \\
&P(I) = I \cdot (V_{15V,max} - I \cdot R24_{min}) \\
&P'(I) = V_{15V,max} - 2 \cdot I \cdot R24_{min} \\
&P'(I) = 0 \rightarrow I = \frac{15.75\ V}{2 \cdot 95\% \cdot 150\ \Omega} = 55.3\ mA \\
&P_Q = 55.3\ mA \cdot (15.75\ V - 55.3\ mA \cdot 95\%150\ \Omega) = 436\ mW
\end{aligned}
$$

436 mW is barely more than the maximum 400 mW the transistor can tolerate.

The maximum power in R24 during a dead short is:

$$P_R = V_{15V,max}^2 / R24_{min} = 1.741\ W$$

2.4.3.3 `analog_current`: Q5

The power dissipation in Q5 for `analog_current` will not exceed:

$$P = (15.75\ V - 0.6\ V) \cdot 20\ mA + 0.7\ V \cdot 0.2\ mA = 304mW$$

The 0.6 V voltage drop is from D6.

2.4.3.4 Digital outputs: Q3, Q4, Q6, Q7, R12, R13, R22, R23

R12 and R13 are chosen to be 47 kΩ and 3.3 kΩ to have a digital output with low dropout (well saturated) with a max load of 100 mA. (The exact calculations have been forgotten.)

R22 and R23 are the same as R12 and R13.

2.4.4 Fixed voltage dividers (resistors and some potentiometers)

Half of these are listed as 22 k, but the actual value doesn't as long as the ratio is correct and they are in a sane range (eg. 10k - 100k).

The pairs (R7, R8), (R9, R10), (R14, R15), (R16, R17), (R18, R19) and (R20, R21) are all 50% dividers with varying requirements of accuracy:

- The ratio between R7:R8 (22k) and R9:R10 (470k) is critical.
- The error from R9:R10 (same as R7:R8) can be calibrated away with P2 plus P3.
- The error from R14:R15 can be calibrated away with P5 and P6.
- The error from R16:R17 can be calibrated away with P5, P6 and P7.
- The ratio R18:R19 (470k) is critical.
- The ratio R20:R21 (22k) is critical.

The pairs (R9, R10), (R14, R15) and (R18, R19) are 50% dividers that need to have a high resistance as the op-amps may in a worst case scenario only be able to sink 12 μA.

Minimum values depends on maximum voltage across the entire divider:

$$12\ \mu A \geq \frac{10\ V - 0.025\ V}{R9 + R10} \rightarrow R9 \geq 416\ k\Omega$$
$$12\ \mu A \geq \frac{2\ V - 0.5\ V}{R14 + R15} \rightarrow R14 \geq 62.5\ k\Omega$$
$$12\ \mu A \geq \frac{10\ V - 0.5\ V}{R18 + R19} \rightarrow R18 \geq 396\ k\Omega$$

Using 470 kΩ for all of R9, R10, R14, R15, R18 and R19 will simplify the BOM and allow for more cherry picking. R14 and R15 could use as low as 68 kΩ

Only the 50% dividers have been selected with fixed resistors, the rest are done with trimmer potentiometers:

P4	1/4 accurate divider	loads signal output (100kΩ)
P5	1/5 accurate divider	loads signal output (100kΩ)
P6	1/5 accurate divider	loads V_{ref} (100kΩ)

The actual value is not critical, but calculations for the TL431 assume P6 is 100k and P4 and P5 are assumed to not cause any noticeable load on the voltage output.
The PCB is designed for `V10-*` footprints for P4, P5 and P6.

2.4.5 G to U gain: P2, P3

P2 and P3 are combined to tolerate the potentially high power dissipation of $I_{LDR,max} \cdot 15\ V = 0.7\ W$. They still need to tolerate half of that each so a couple of larger cermet trimmer potentiometers have been chosen. `T910Y-*` or `T910W-*` are rated for 0.5 Watts, have the screw on an accessible side, and also has the benefit of a low $\pm 100\ ppm/°C$ temperature coefficient.

The total range of resistance needs to include 320Ω to 8kΩ. The PCB is designed for two `T910Y-*` in series. Preferrably `-5K` (5kΩ) but can be larger.

2.4.6 U to I gain: P7

P7 is used as a 125 ohm resistor. Max power dissipation in the circuit is $(20\ mA)^2 \cdot 125\ \Omega = 50\ mW$. The PCB is designed for a `V10-*` footprint. Needs to be `V10-250` or larger resistance.

2.4.7 Comparator output: R25, P8, P9

P8 sets the digital output threshold level. No specific value required but should be significantly smaller than P9. The PCB is designed for a `P10-*` footprint. 10 kΩ is a nice round value.

P9 sets the digital output's hysteresis. No specific value required but should be significantly larger than P8. The PCB is designed for a `P10-*` footprint. 1 MΩ is a nice round value that is a lot larger than 10 kΩ but still not insanely high.

R25 sets the maximum amount of hysteresis to the digital output and also limits the current from V_{ref} to ground, V_{ref} to V_S and V_S to ground that goes through the opamp should P9 be set to zero.
47 kΩ gives an insane amount of hysteresis while also more than sufficiently limiting the current. Assuming the output from the opamp is either 20 volts or zero and that P9 is set to 50%, it will change the trigger level:

$$trig_{norm} = ref/2 = 50\%$$
$$trig_{high} = \frac{\frac{ref}{5k} + \frac{0}{5k} + \frac{8ref}{33k}}{\frac{1}{5k} + \frac{1}{5k} + \frac{1}{33k}} = 87.9\%$$
$$trig_{low} = \frac{\frac{ref}{5k} + \frac{0}{5k} + \frac{0ref}{33k}}{\frac{1}{5k} + \frac{1}{5k} + \frac{1}{33k}} = 47.5\%$$

With P8 set to 50% and P9 set to max hysteresis the actual trigger level will be 67.7% and the hysteresis will be ±20.2%.

2.4.8 7815CP circuitry

The 7815 datasheet suggests a 100 nF bypass capacitor on output (C5) and a 330 nF on input (C4), but since there are no 330 nF in E3 a 470 nF (or even a 220 nF depending on the layout) can be used intead.

The 7815 needs a heatsink because it supplies up to 87 mA at a voltage drop that can be as high as $29\ V - 14.25\ V = 14.75\ V$ and up to 8 mA quiescent current.

The 15 V rail exists to save three transistors from the very same fate. Max power dissipation is 1.52 W.

Maximum power consumption:

$$
\begin{aligned}
&V_{S,max} = 29\ V \\
&V_{min} = 14.25\ V \\
&I_{q,max} = 8\ mA \\
&I_{O,max} = I_{analog\_voltage,max} + I_{analog\_current,max} + I_{LDR,max} = (20 + 20 + 47)\ mA \\
&P_{max} = V_{S,max} \cdot I_{q,max} + (V_{S,max} - V_{min}) \cdot I_{O,max} = 1.52\ W
\end{aligned}
$$

`analog_voltage` can supply more than 20 mA if shorted (up to 100), but since the 7815 has over temperature protection there will be no permanent damage.

A small heatsink such as the 6390B is required for operating correctly.

Assuming the 6390B will be used, or any other 17.4 °C/W heatsink:

$$
\begin{aligned}
&T_{A,max} = 70\ ^\circ C \\
&T_{J,max} = 125\ ^\circ C \\
&R_{\theta JC} = 5\ ^\circ C/W \\
&R_{\theta SA} = 17.4\ ^\circ C/W \\
&P = 1.52\ W \\
&P \cdot (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \leq T_{J,max} - T_{A,max} \\
&\rightarrow R_{\theta CS,max} = \frac{T_{J,max} - T_{A,max}}{P} - R_{\theta JC} - R_{\theta SA} \\
&R_{\theta CS,max} = \frac{55\ K}{1.52\ W} - 22.4\ K/W = 13.7\ K/W \\
&T_{J-A,max} = P \cdot (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) = 34\ ^\circ C + 1.52\ W \cdot R_{\theta CS}
\end{aligned}
$$

The thermal interface material needs a conductance of at least 73 mW/K (resistance less than 13.7 K/W), which sounds reasonable.

The die temperature will (at full load) be more than 34 °C hotter than ambient, which gets very hot at 70 °C ambient.

Due to board size limitations, the 6390B has been used on the PCB layout instead of the better performing SK104 or SK129.

2.4.9 TL431 circuitry

U1 (TL431) requires a minimum cathode current of 400 μA to operate correctly. The load on V_{ref} consists of R5+P1+M1 (7.8 kΩ), P6 (100 kΩ), P8 (10 kΩ), R25* (47 kΩ) and U6 (which actually sources current).

$$I_{min} = I_{K,min} + \frac{2.5\ V}{7.8\ k\Omega} + \frac{2.5\ V}{100\ k\Omega} + \frac{2.5\ V}{10\ k\Omega} + \frac{2.5\ V}{47\ k\Omega} = 1.05\ mA$$

Assuming a 5% tolerance and 250 mW power limit:

$$I_{headroom} = \frac{(19 - 2.5)\ V}{1.05R} - I_{min}$$
$$P_{headroom} = 250\ mW - \frac{(29\ V - 2.5\ V)^2}{0.95R}$$

Resistance (kΩ)	**current headroom (mA)**	**power headroom (mW)**
2.2	6.09	**FAIL**
3.3	3.71	25
4.7	2.29	92
6.8	1.26	141
10.0	0.52	176
15.0	**FAIL**	200

4.7 or 6.8 kΩ is a good choice.

2.4.10 Miscellaneous

C1 is a largeish ceramic or film capacitor to be placed as close to the supply input as possible to soak up noise and hopefully any ESD at the connector.
C2 is a 10 μF electrolytic bulk capacitor to be places wherever it fits on the board.

C12 and C13 provide bypass for digital outputs, each of the outputs should also have ground terminals close to respective capacitor. Due to the high current these should have a decent amount of capacitance.
Each output also has an optional back-EMF diode (D4 and D5). Doesn't really matter for a prototype as any inductive load should have it on the load side anyway. *Update:* D4 and D5 should preferrably be schottky diodes or very fast diodes. 1N4148 has been chosen which hopefully will be adequate.

D3 needs to have lowish leakage as the R9/R10 divider is designed for an op-amp that (in the worst case) may be unable to sink more than 12 μA. A leakage below 120 nA would result in less than 1% error.
A 1N4148 has less than 15 nA leakage at the full 6.25 volts. 0.1% error.

D6 exists to prevent U10 to back feed the 15 V rail through the base-collector junction of Q5 if the output is disconnected. Speed is not a concern. Any normal diode will do fine.

C14 was added experimentally to fix some ringing found in LTspice. 1pF was too little, 10 pF did the job. C14 may or may not be needed in the real circuit and the capacitance required may be something else.
It must not be too large. The rise time of the LDR is 20 ms, C14 must not cause the sensor to be slower: the time constant of C14 and R9 should be at least an order of magnitude lower than 20 ms. $20\ ms/470\ k\Omega/10 = 4.2\ nF$
It probably doesn't have any other adverse effects than being a low pass filter, so maybe 100 pF to be on the safe side.

3 Simulations

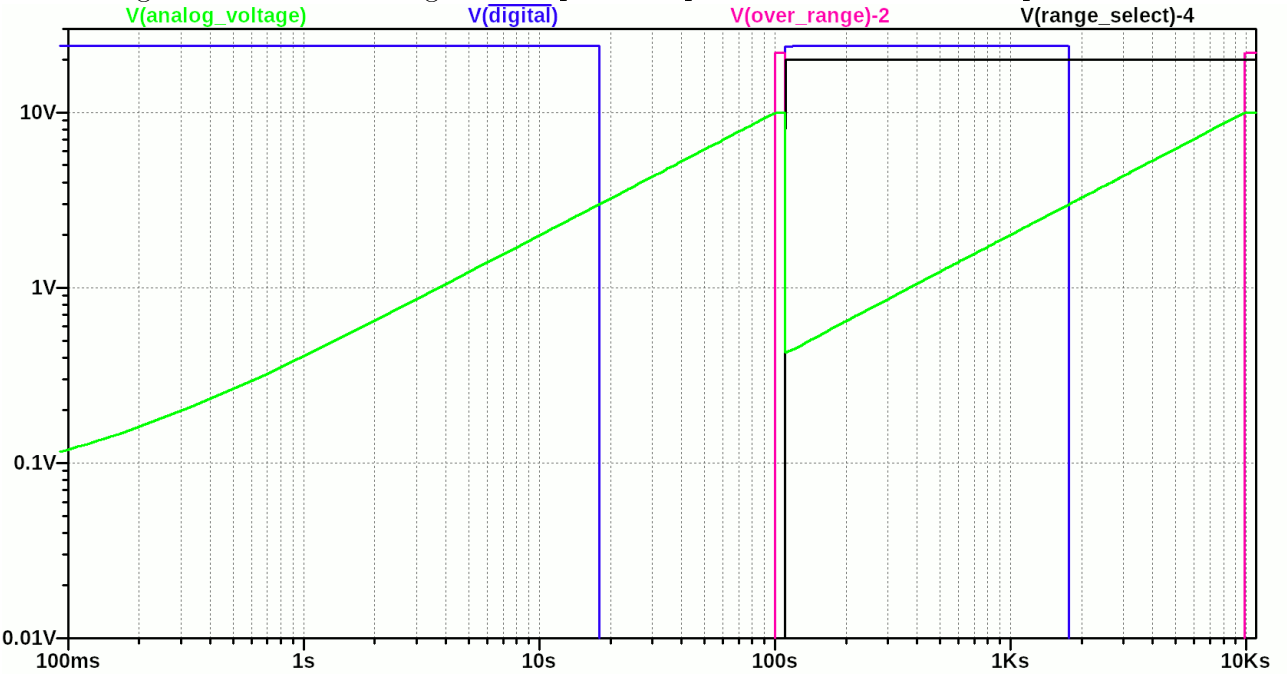
The simulations are transient simulations using time as a variable for calculating LDR resistance. The simulated illuminance starts at 1 Lux and increases by 10 Lux/s.

$$E = 1\ Lux + t \cdot 10\ \frac{Lux}{s}$$

Do note that this causes some visible distortion as 100 ms corresponds to 2 Lux rather than 1.

3.1 Default simulation

Various signals when simulating the complete LTspice circuit with default parameters:



1 Lux to 110 000 Lux log scale, 0.01 V to 30 V log scale.

This is the simulation of all external signals except `analog_current` in a log-log scale.

- `range_select` goes from low to high at 1100 Lux (110 s)
- $\gamma = 0.7$
- $R_{10} = 10\ k\Omega$
- $level = 2\ k\Omega$ (20% trigger level for comparator output)
- $hyst = 100\ k\Omega$
- Load on `analog_voltage` is 500Ω, the maximum allowed
- Digital signals offset to avoid overlap.

3.2 Supply voltage independence

Analog voltage and current, and `over_range` at varying voltages overlapped.

The analog signals should overlap as one black line. `over_range` is separated as it is a digital signal that goes only as high as the supply voltage.

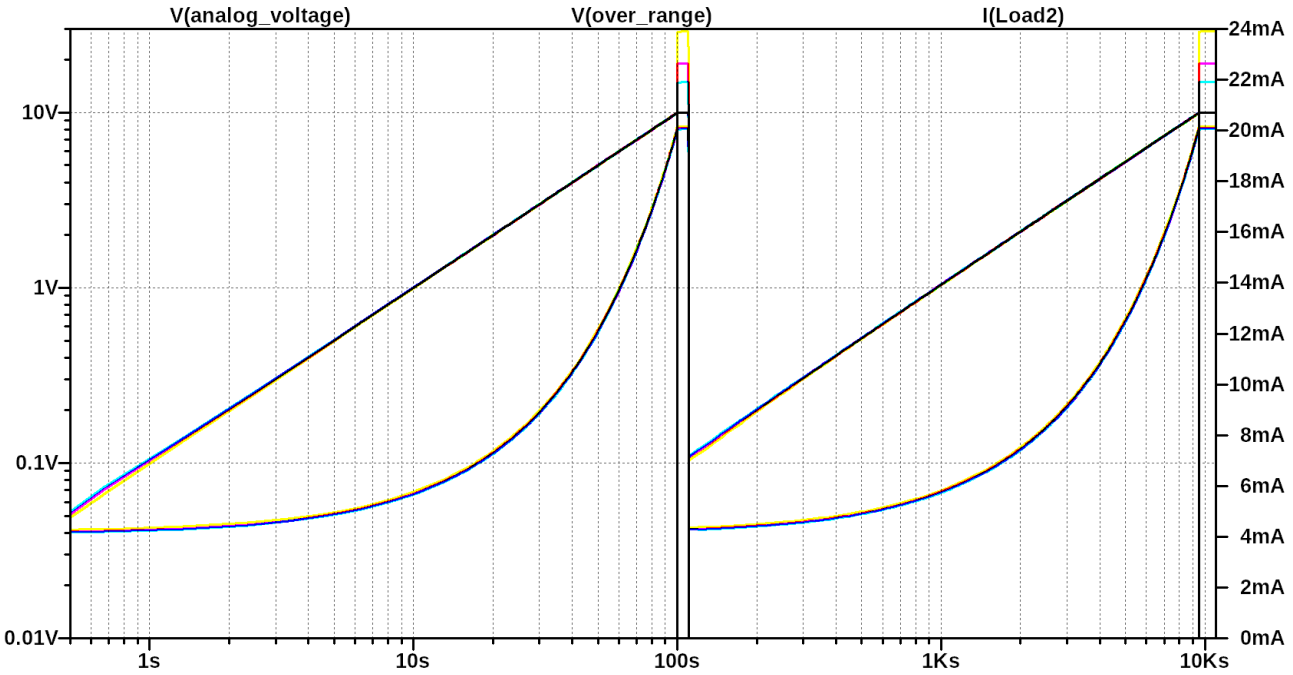
Cyan component	15 V *
Magenta component	19 V
Yellow component	29 V

* The 15V is specific to the simulated circuit. The LM358 may have up to 4 volts drop in the worst case and the 7815 can output as low as 14.25 V. The LTspice simulation uses generic (ideal) op-amps which are rail-to-rail. 15 V in the simulation is equivalent to 19 V in real life with the worst case LM358s and 7815.

For maximum stress at lower supply voltages:

- 20 mA on voltage output
- 10 V on current output
- $\gamma = 1$ and $R_{10} = 8\ k\Omega$

`range_select` is used just like in the default simulation, but the trace is not shown to remove clutter. The curvy trace is the current.



6 Lux to 110 000 Lux (500 ms to 11 ks)

There seems to be an about 6% error on the voltage below 10 Lux, but it becomes imperceptible after 30 Lux. Rather counter-intuitively, a lower supply voltage yields a higher signal voltage.

The current output has very little error.

3.3 Power/current draw

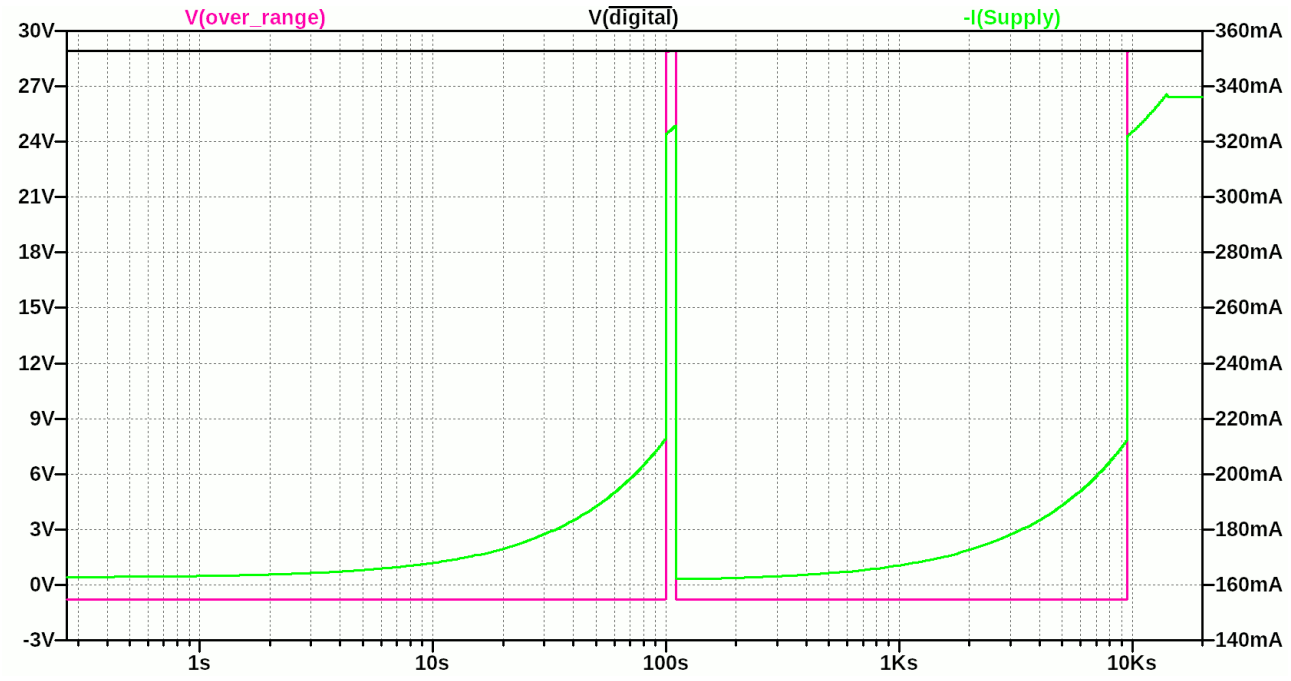
For maximum current consumption:

- 20 mA current draw on `analog_voltage` and 100 mA on each of the digital outputs
- Illumination up to 200 000 Lux
- $\overline{\texttt{digital}}$ forced to be always high
- $\gamma = 1$ and $R_{8\ k\Omega}$ for maximum current through the LDR.
- Simulation is run at 29 V
- Simulation has current sources to account for the quescient current in the 358s and the 7815 (in `7815.asc`).

level and *hyst* have been set up to cause the comparator to latch up with a trigger level above 100% to cause both digital outputs to be high simultaneously:

$$level = 8\ k\Omega$$
$$hyst = 0\ k\Omega$$
$$V_{trig,high} = \frac{\frac{25\ V}{47\ k\Omega + hyst} + \frac{2.5\ V}{10\ k\Omega - level} + \frac{0\ V}{level}}{\frac{1}{47\ k\Omega + hyst} + \frac{1}{10\ k\Omega - level} + \frac{1}{level}} = 2.76\ V$$

At the beginning $\overline{\texttt{digital}}$ will go high because near zero illuminance is below the trigger level. As soon as the output goes high the actual trigger level will be bumped to 110%.



`range_select` is used just like in the default simulation, but the trace is not shown to remove clutter.

The two digital signals are monitored to ensure they both are high.

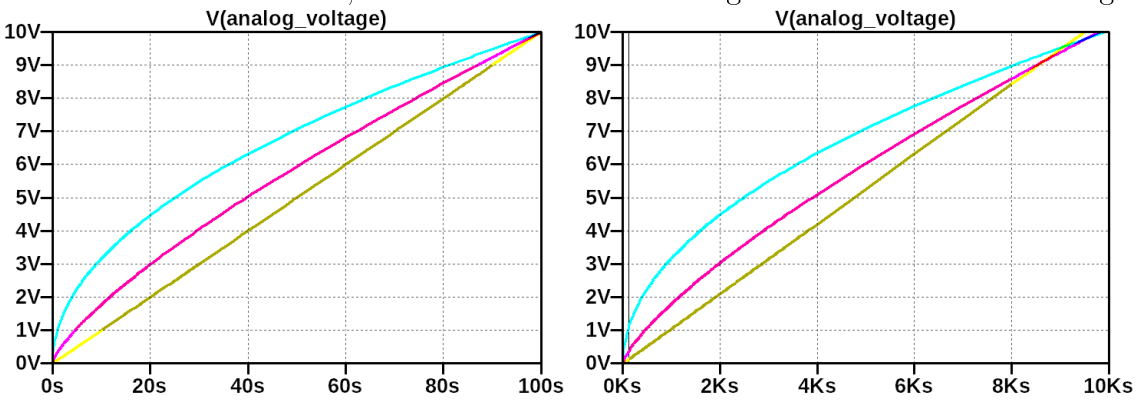
Current consumption is below 340 mA, of which 220 mA is spent on voltage outputs.

3.4 Transfer function

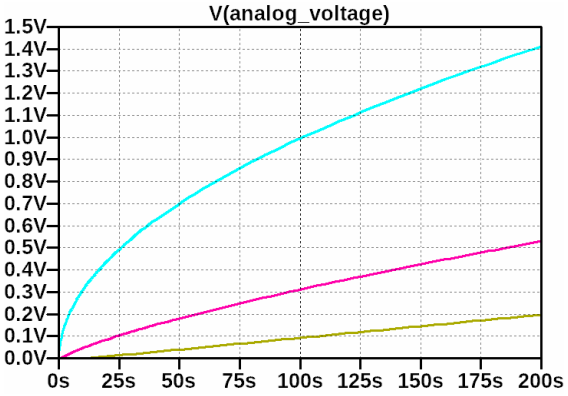
Curves of the transfer function (light to voltage) through the range of gamma characterstics:

Cyan	$\gamma = 0.5$
Magenta	$\gamma = 0.75$
Yellow	$\gamma = 1$

0 to 1000 Lux on the left, 0 to 100 000 Lux on the right with a thin line marking 1000 Lux:



0 to 2000 Lux in the 0 to 100 000 Lux scale, at 1000 Lux (100 s) the voltage would be 10 V in the 1000 Lux scale:



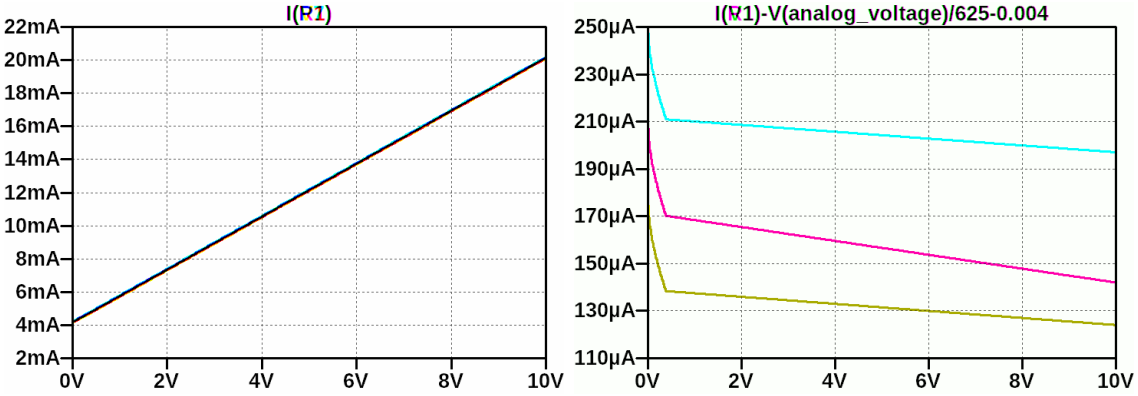
The 2000 Lux and 100 000 Lux graphs were taken with `range_select` held to 24 V the entire time, and the 1000 Lux graphs with 0 V.

3.4.1 Current output

Current output through various loads:

Cyan	short
Magenta	250 Ω
Yellow	10 V

Simulated U to I transfer on the left, deviation from intended current on the right:

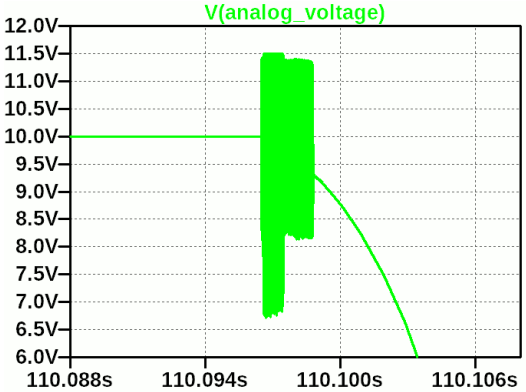


The voltage to current simulation was done using only the U-to-I part with a DC analysis. V_S is 24 V.

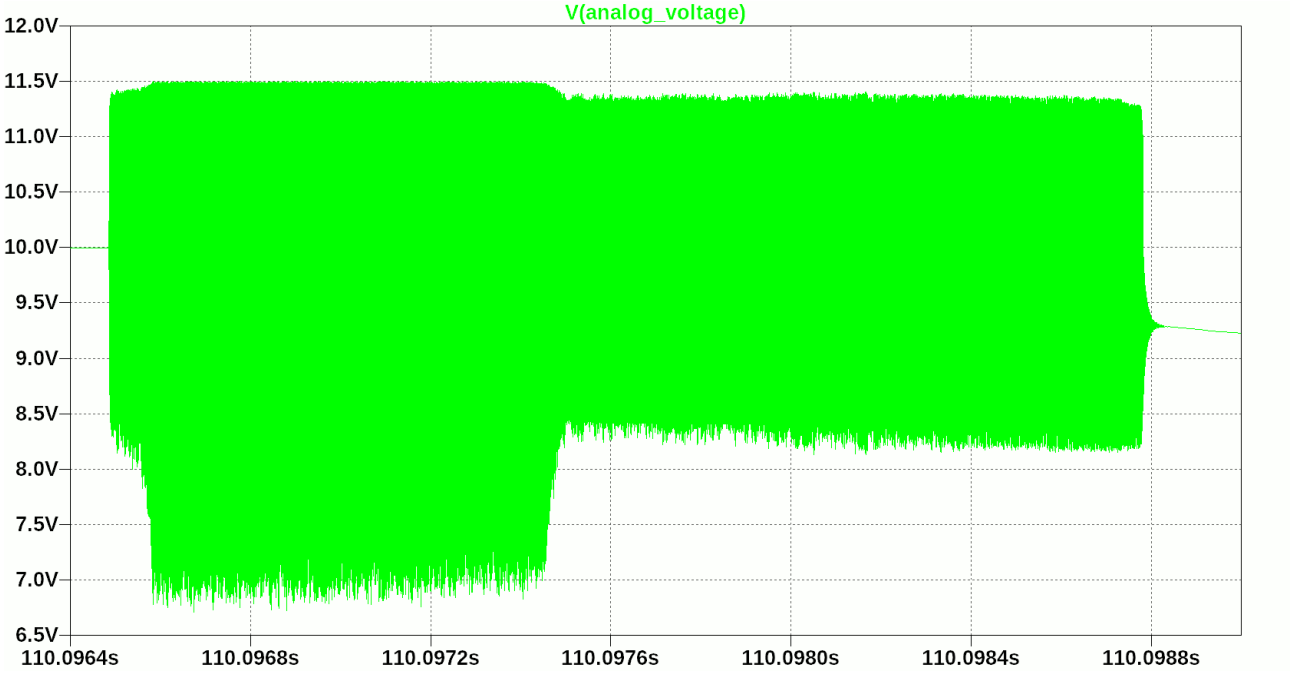
3.5 Ringing without C14

Very picky. Works fine with 24 V or with a 120 seconds long simulation. Using 19 V and `.tran 200` is sufficient to cause ringing in the simulation.

Ringing occurs when the differential signal falls back to below 10 volts:

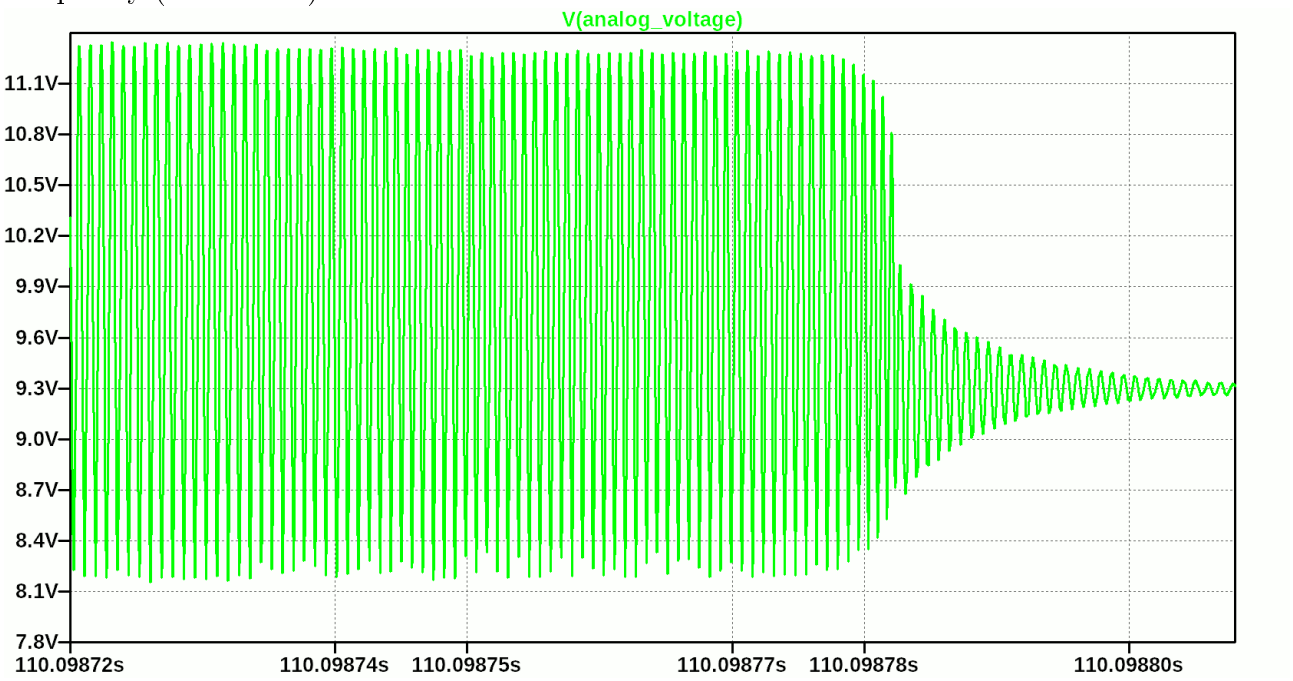


Amplitude and duration:



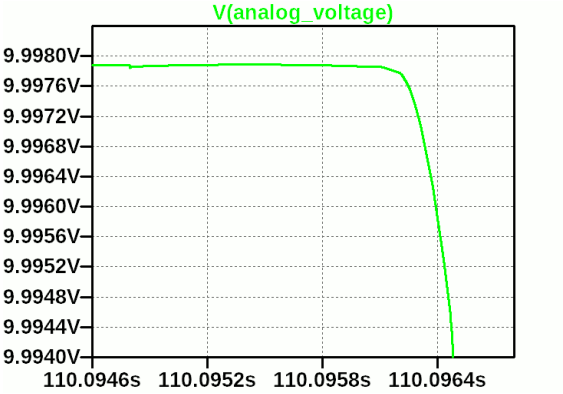
4.75 volts peak to peak at worst, at or above 3 V p-p for about 2.3 milliseconds. There also seems to be something clamping it to 11.5 volts.

Frequency (at the end):

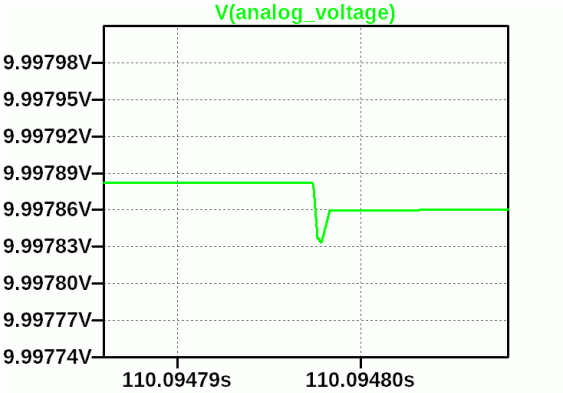


Looks to be about 1.25 MHz between ...770 and ...780. It may look like the frequency suddenly decreases but that's not the case.

Adding C14 removes the ringing almost completely:



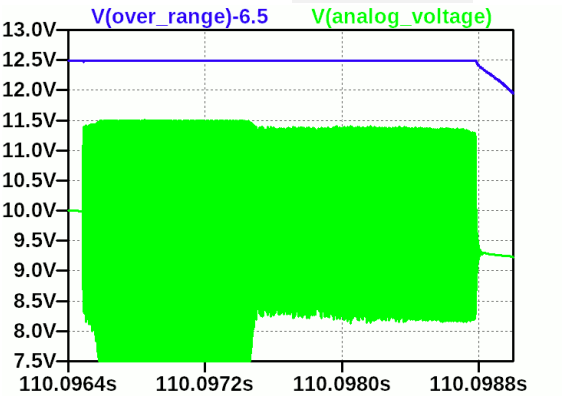
Zooming in on the tiny blip at 110s 94ms 798μs:



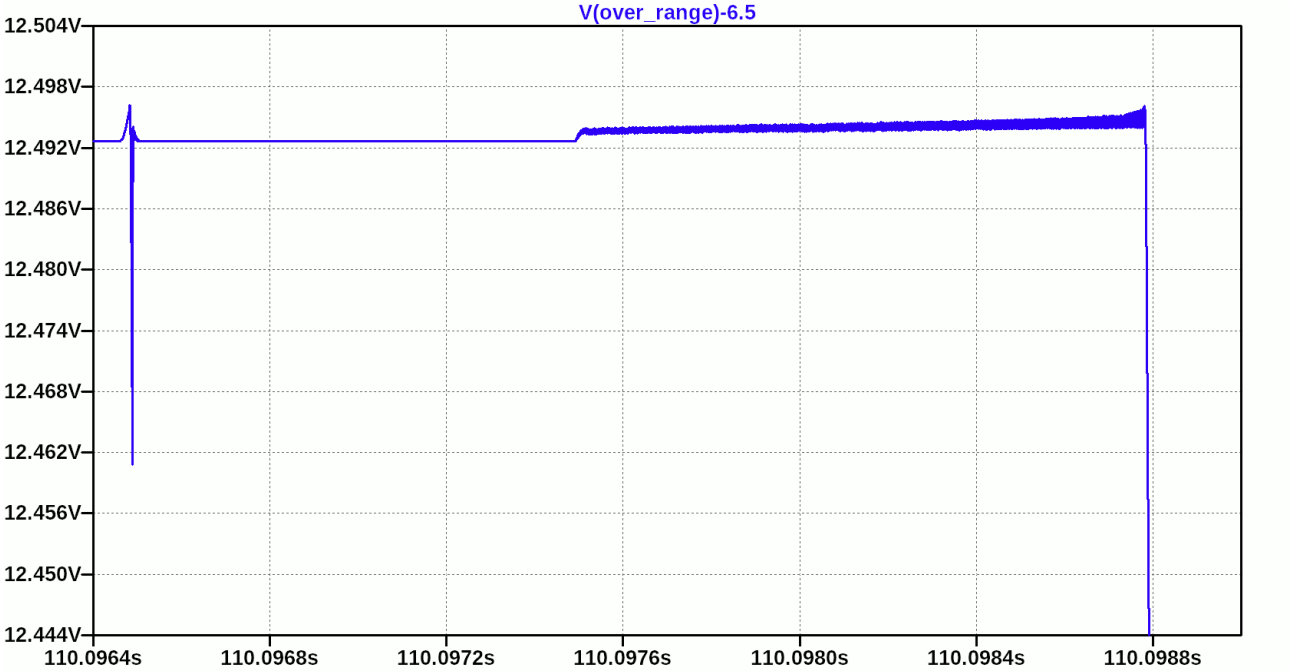
The amplitude appears to be about 50 μV p-p. Looks like one cycle of about 500 kHz to 1 MHz.

3.5.1 Ringing on `over_range`

A very small blip on `over_range` at the start of the ringing on `analog_voltage`:

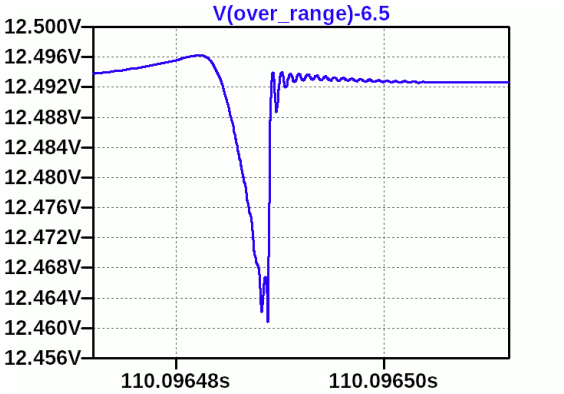


The blip and some delayed ringing visible when zooming in:

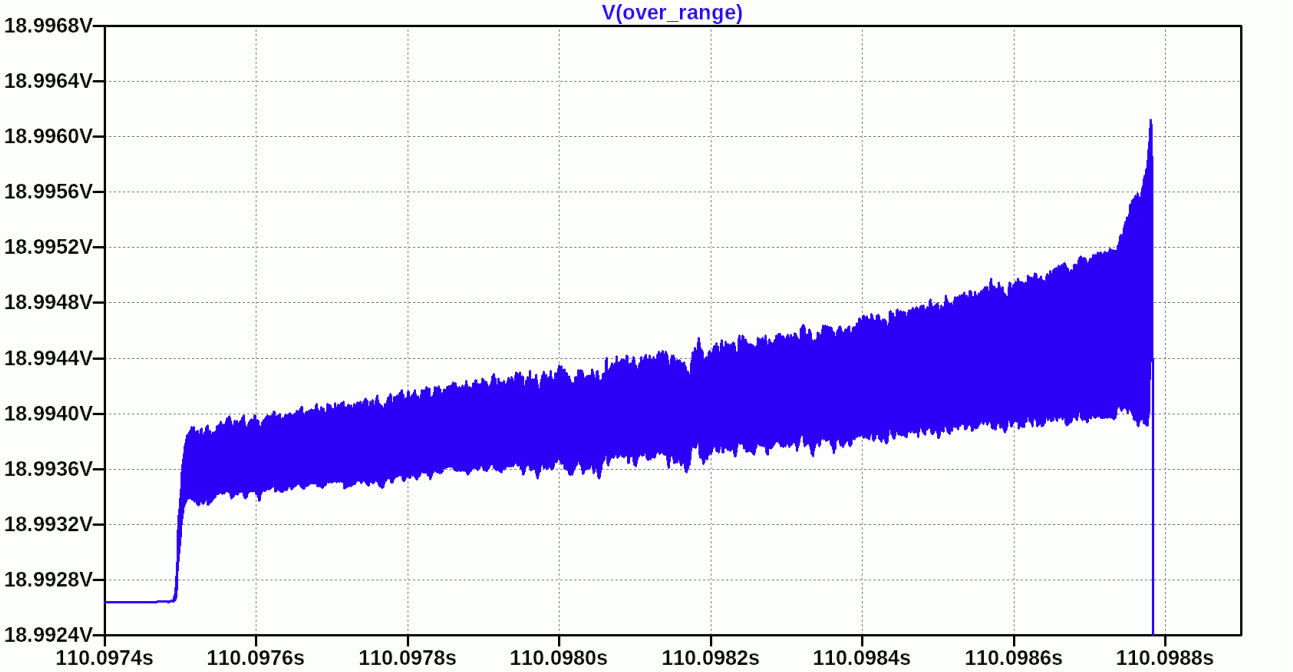


It appears that whatever clamping happened at 11.5 V on `analog_voltage` kept the ringing silenced.

The blip zoomed in:



The ringing zoomed in:

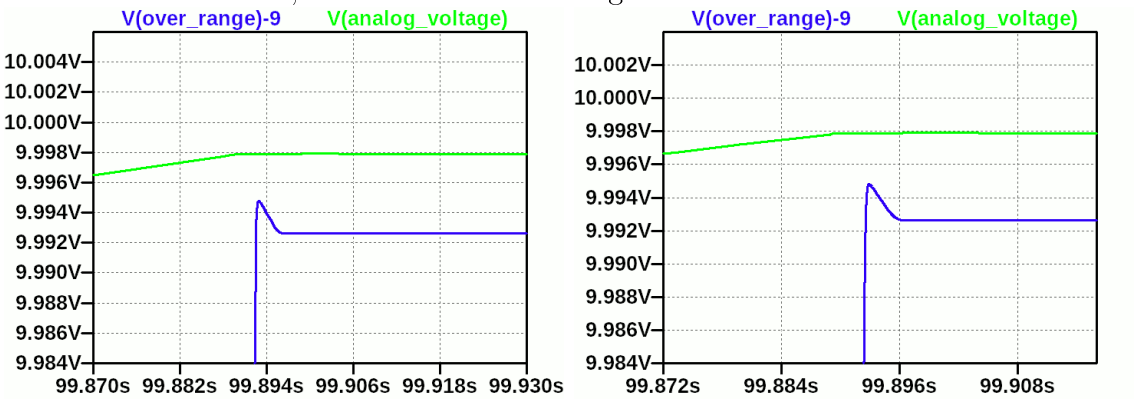


3.5.2 Rising edge

Could slowing down U5 cause problems on the rising edge?

Update: **This simulation was done with C14 at 10 pF, but it should have been 100 pF.** Because of this mistake, this simulation may be faulty.

With C14 on the left, without C14 on the right:



There is some overshoot but only on the digital signal and independent of the addition of C14.

Intentionally slowing down U5 does not seem to cause any issues.

3.6 Simulation parameters

These are the parameters set in the complete LTspice schematic.

- Some of the loads can vary between constant resistance, constant current and constant voltage
- PWL refers to a waveform function that is 0 V from 0 Lux to 1 100 Lux and then switches to 24 V
- A star indicates that it's not a fixed value, see the section for the specific simulation for details
- `.tran` sets the transient analysis time because the LDR is simulated through time: $E = 1\ Lux + t \cdot 10\frac{Lux}{s}$

	Default	Voltage	Power	Transfer	C14
`supply`	24 V	*	29 V	24 V	19 V
`LDRy`	0.7	1.0	1.0	*	0.7
`LDR10`	10 kΩ	8 kΩ	8 kΩ	10 kΩ	10 kΩ
`load1`	500 Ω	20 mA	20 mA	500 Ω	500 Ω
`load2`	1 Ω	10 V	0 V	1 Ω	1 Ω
`load3`	1 MΩ	1 MΩ	100 mA	1 MΩ	1 MΩ
`load4`	1 MΩ	1 MΩ	100 mA	1 MΩ	1 MΩ
`level`	2 kΩ	2 kΩ	8 kΩ	2 kΩ	2 kΩ
`hyst`	100 kΩ	100 kΩ	0.01 Ω	100 kΩ	100 kΩ
`.tran`	11000	11000	20000	*	200
`range_select`	PWL	PWL	PWL	*	PWL

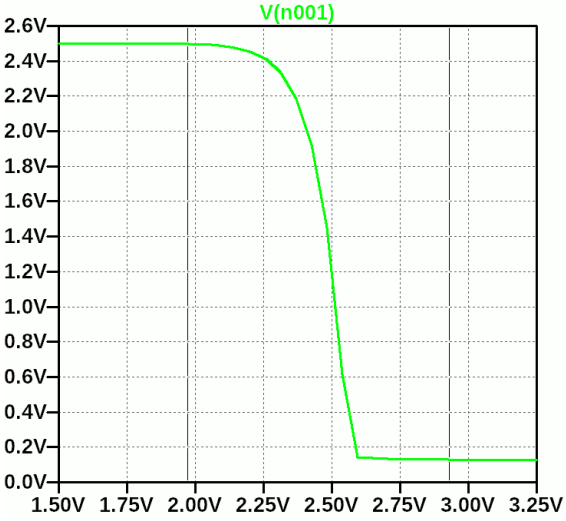
3.7 `range_select`

It is not known how M1 (BS170) will behave at low input voltages. It will likely conduct far too hard at its threshold.

This is a simulation using BSS123 which appears to be somewhat similar.

Parameter	**BS170**	**BSS123**	**unit**
max I_{DSS} (25 °C)	0.5	1	μA
max I_{DSS} (125 °C)	-	60	μA
test V_{DS}	25	100	V
max $R_{DS(on)}$	5	6	Ω
typ $R_{DS(on)}$	1.8	1.2	Ω
test V_{GS}	10	10	V
min $V_{GS(th)}$	0.8	0.8	V
typ $V_{GS(th)}$	2.0	1.7	V
test I_D	1	1	mA
test V_{DS}	V_{GS}	V_{GS}	V
min g_{FS}	-	0.08	S
typ g_{FS}	0.2	0.8	S

P5 has been adjusted for 5% of 2.5 V. The output voltage should stay at either 2.5 V or 125 mV. Y-axis is the output voltage, X-axis is `range_select`:

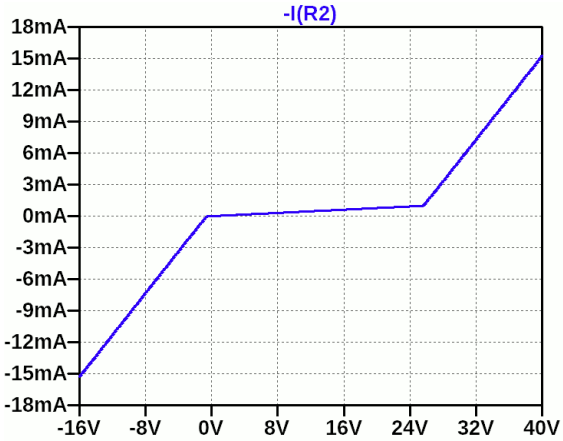


For a typical BSS123 and no tolerance issues on the resistors, etc:

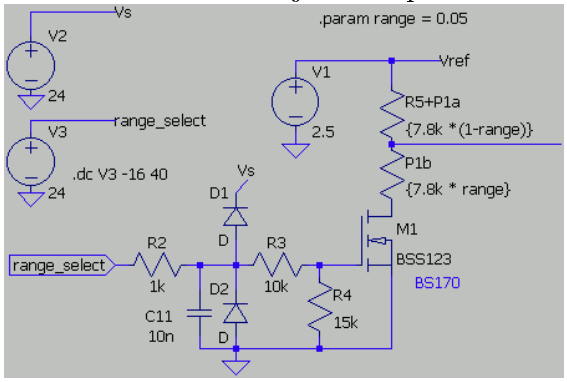
$V_{low,max}$	1.96 V
$V_{high,min}$	2.94 V

The saturation voltage of a BJT is probably low enough to not cause any issues.

Input current draw (typical, at nominal resistance and $V_S = 24\ V$):



This simulation used just the part that divides the reference voltage for the two different scales.



3.8 Hysteresis for `digital`

Graphs of low and high trigger voltage through all parameters. If the high value exceeds 10 V, the comparator will lock up if it ever gets darker than the low trigger level.

P8 sets the level between 0 and 10 V. P9 set the hysteresis between 1 MΩ and 0 Ω, P9 is always in series with 47 kΩ.

These are not actual simulations, but graphs for the functions listed for `digital` in section 6.3 - Transfer functions.

The LM358s limited ability to sink current at low output voltages has not been considered, but most of the hysteresis is on the upper value anyway.

3.8.1 Logarithmic scale for P9 values

To get R25+P9 to be 47 kΩ to 1047 kΩ on a logarithmic scale

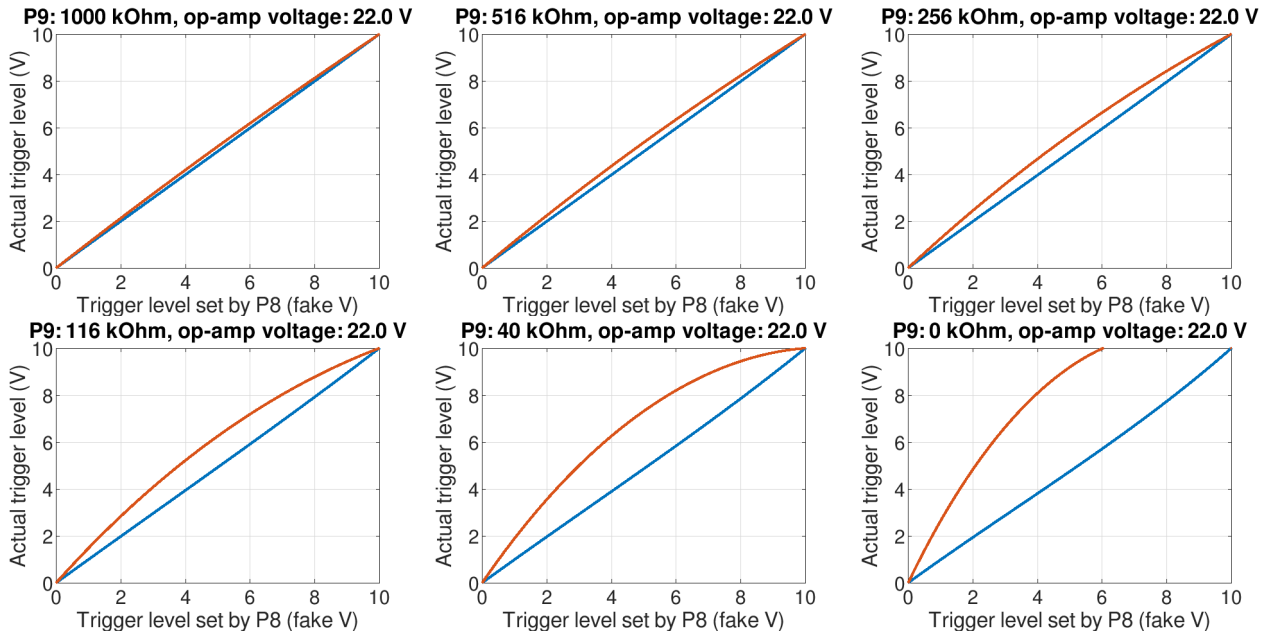
$$x = \sqrt[n-1]{\frac{1047\ k\Omega}{47\ k\Omega}}$$
$$R_i = 47\ k\Omega \cdot x^i - 47\ k\Omega$$

Where n is the number of levels and i is from 0 to $n-1$. R_i is the value of P9.

This is what has been used to calculate the fixed values for P9 for the graphs below.

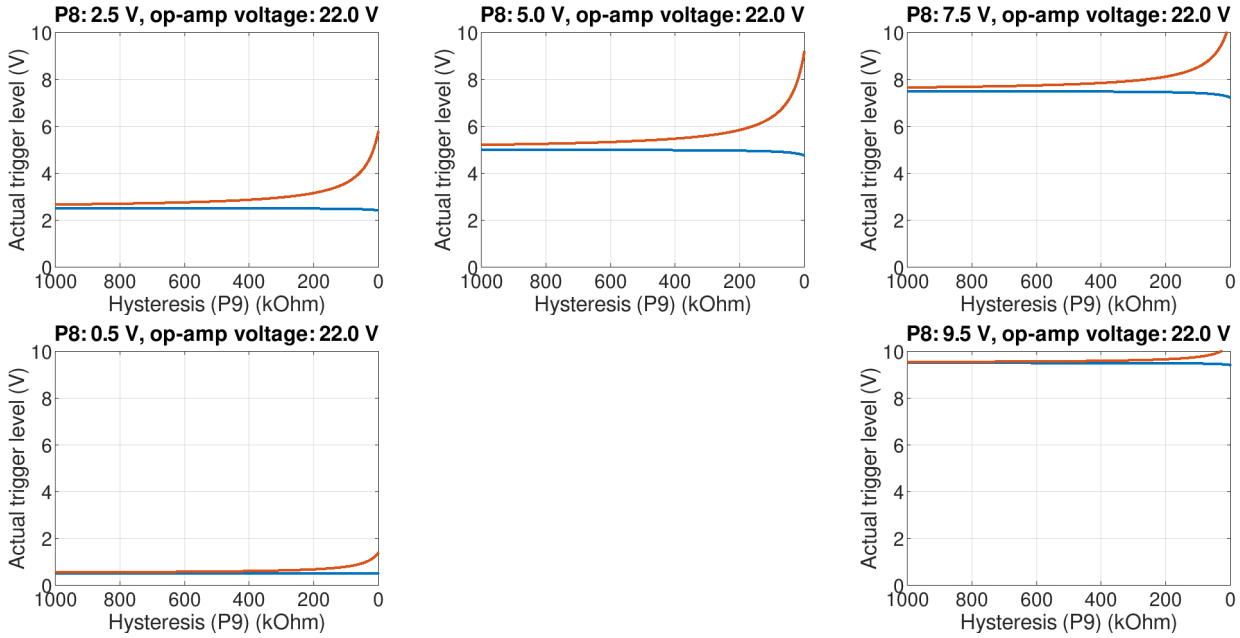
3.8.2 Set level vs actual level, different levels of hysteresis

Op-amp high output voltage is 22 V. Six levels of hysteresis.



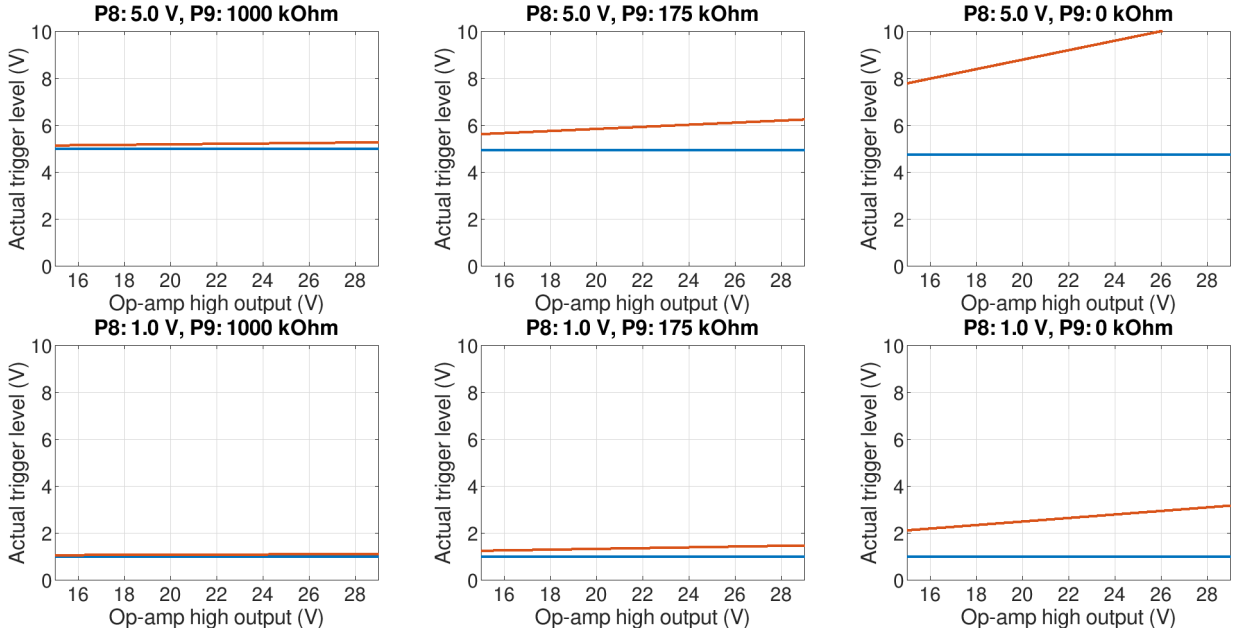
3.8.3 Hysteresis control, different set levels

Amount of actual hysteresis vs P9 position at five different set trigger levels.



3.8.4 Hysteresis vs op-amp output voltage

Effects of supply voltage and op-amp drop out on hysteresis. Set voltage at 5 V for high impact and 1 V for low impact.



4 EMC considerations

EMC was not expected to be much of a concern due to the slow speed of the LDR. Potential exceptions are the digital outputs, power supply decoupling and common mode noise from long external wires.

All ICs have their recommended bypass capacitor with a loop as small as feasible. The ground "plane" has plenty of coverage but unfortunately contains large islands.

C12 and C13 are bypass capacitors for the digital outputs. As they are designed to tolerate quite high current draw large capacitors may be required, but as the load isn't expected to be very fast a low-ESR electrolytic capacitor may be sufficient.
For the prototype anything with more than 100 nF capacitance and lower ESR than a standard aluminium electrolytic will do fine.

If common mode noise turns out to be a problem, cables can be few turns through (a) ferrite ring(s). For power supply decoupling C1 and C2 is used directly at the 24V input.

The only digital input `range_select` has a 26 kΩ input resistance to ground and a rather low upper limit for logical low voltage, if connected with a long wire it should be actively driven low (as opposed to going high impedance) to prevent mains hum pick up.
R2/C11 exist primarily for ESD protection for the MOSFET but also causes a first order 16 kHz low pass filter.

The range limiter caused some extreme ringing (11 V peaks on a 10 V limiter) in LTspice as `range_select` went high, but this was mitigated by the addition of C14, a 100 pF capacitor from output to inverting input on U5/IC3A.
Similar ringing was noticed on the comparator but it apparently went away with the addition of C14 earlier.

5 Construction

5.1 Mechanical construction

The PCB has been designed for the 1598B enclosure. The front panel can easily accomodate access (by removing it) to a bunch of connectors and two trimmer potentiometers for the comparator output.

A PCB front panel (max 1.65 mm thickness) could be used to add screw terminals, but no such panel has yet been planned.

The top edge of the PCB (where the I/O and power connectors are) will line up with the front panel. There should be enough space to connect and disconnect the Molex connectors (2 pin, 2.54 mm, not the PC kind).

Molex headers have been chosen as connectors beccause they were the easiest to do in Eagle. They are installed backwards to make it easier to access the clip through the front opening.

The LDR is intended to be installed in a short tube with semi-permanantly attached wires to the circuit (10cm to 30cm ish). Keeping the electronics at a slight distance from the LDR allows the light sensing part to be less clunky. Permanent attachment or another low resistance connection may be better for the LDR depending on its conductance at maximum brightness.

Nothing has been formally planned for the LDR, but the intent is to mount it (glue it on the backside) in a hard thin tube, eg. the outer shell of a ballpoint pen.

5.1.1 Front panel

No PCB front panel has been designed. But an important feature is an optional pull-up resistor for `range_select`.

External wires can connect to PCB mount screw terminals or any other easy to use connectors.

The front panel itself can either be directly wired to the main PCB or have surface mount wires leading to seven two pin molex connectors.

5.1.2 PCB fitment

Blueprints for the 1598B case

The largest rectangular board that can fit is 100.98 mm (*1) (side facing panel) by 122.30 mm. The PCB's dimensions were 100.97 mm by 82.55 mm and the edges can be filed down if needed.

The PCB has been shrunk: 25 mils were removed from the left and 25 mils from the right edge making the board only 99.70 mm wide which will fit more easily into the case. All calculations here, however, still assume that the board is 100.97 mm.

Mounting holes should be at:

Hole	mm from left edge	mm from top edge	calculations
Upper left	12.29	29.00	2, 3
Upper right	88.69	29.00	4, 3
Middle left	12.29	61.15	2, 5
Middle right	88.69	61.15	4, 5
Bottom left	12.29	93.30	2, 6
Bottom right	88.69	93.30	4, 6

"Actual" hole locations:

Hole	mm from left	mm from top	error (μm) (*7)
Upper left	12.32	28.96	50.0
Upper right (*8)	88.65	28.96	56.7
Middle right	88.65	61.09	72.1

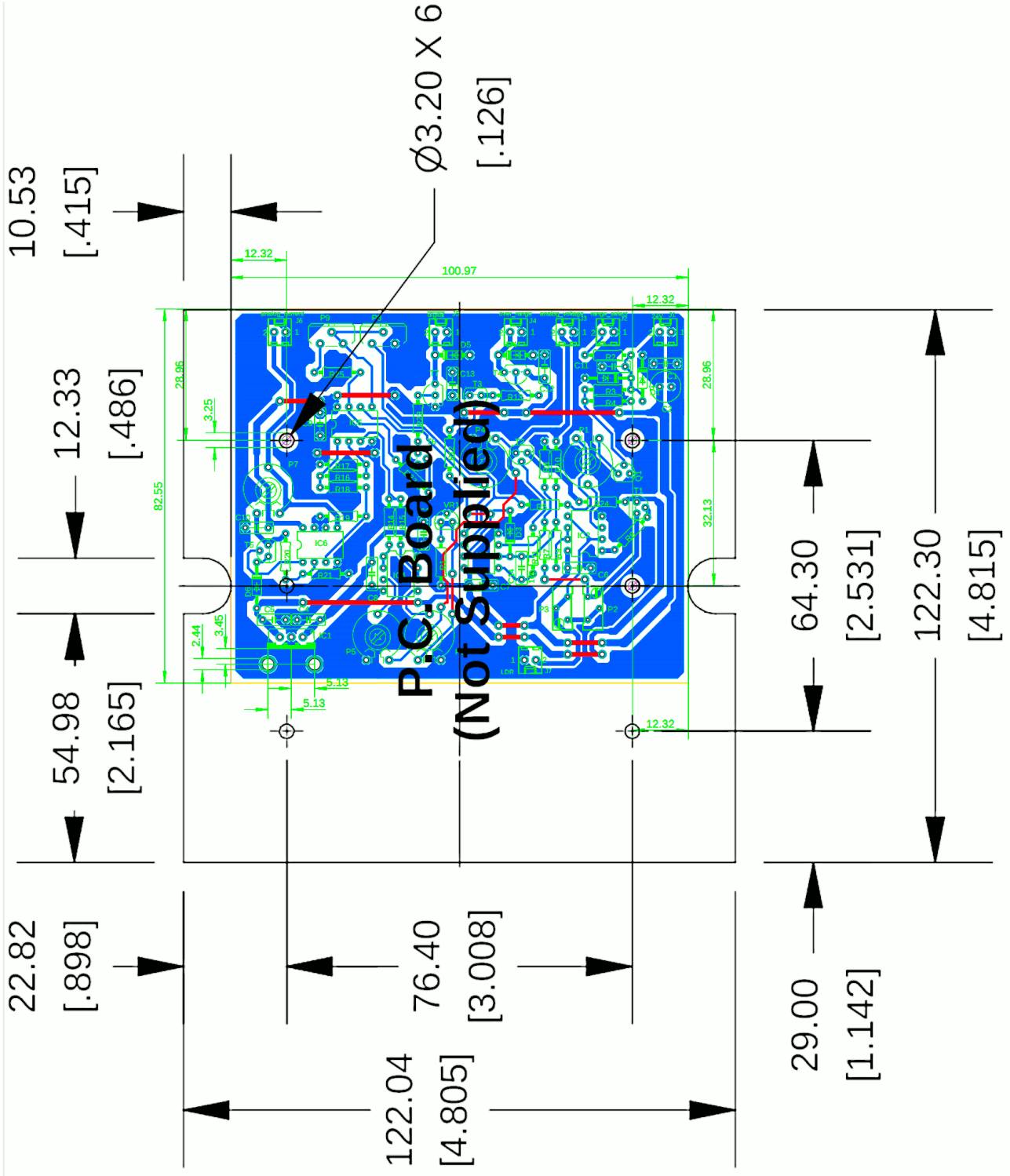
The holes are 4 mm in diameter. The screws are about 3.5 mm, and there is an additional 0.15 mm increment to the required hole diameter due to the above errors. Minimum diameter is 3.65 mm.

$$122.04 - 2 \cdot 10.53 = 100.98 \tag{1}$$
$$100.98/2 - 76.40/2 = 12.29 \tag{2}$$
$$(122.30 - 64.30)/2 = 29.00 \tag{3}$$
$$100.98 - 12.29 = 88.69 \tag{4}$$
$$29.00 + 64.30/2 = 61.15 \tag{5}$$
$$61.15 + 64.30/2 = 93.30 \tag{6}$$
$$err = \sqrt{(\Delta x)^2 + (\Delta y)^2} \tag{7}$$
$$100.97 - 12.32 = 88.65 \tag{8}$$

The hole diameter for the heatsink is 2.5 mm. The pins are 2.36 mm in diameter. The spacing is supposed to be 10.29 mm but is approximately 10.26 mm due to rounding errors.

Update: The hole diameters for the heatsink turned out to be a bit too small. This error will not be corrected here.

Visually inspecting that the board will fit:



Changes since visual inspection:

- R20 has been moved 20 mils to the right and 60 mils down.
- Mounting holes have been enlarged from 3.35 mm to 4 mm.
- The left and the right edge have both been moved inward by 25 mils.

5.2 PCB layout

The schematic has been recreated in Eagle so a PCB layout could be created.

On the following pages are printouts of the schematic and a top view of the layout.

Differences between LTspice and Eagle:

LTspice	LDR	M1	Q*	U1	U2	U3	U5	
Eagle	J7 (see note)	Q1	T*	VR1	IC1	IC2A	IC2B	
LTspice	U5	U6	U7	U8	U9	U10	U11	U12
Eagle	IC3A	IC3B	IC4A	IC4B	**IC5A**	IC6A	IC6B	**IC5B**

*) The LDR is connected through a Molex header on the board. No LDR is in the Eagle schematic or board layout.

Design rules:

Signal trace width	20 mil
Signal trace clearance	8 mil
Ground trace width	40 mil
Ground trace clearance	20 mil
Polygons	See notes
Power trace width	40 mil
Power trace clearance	20 mil
Pad/via clearance	20 mil
Copper - edge clearance	30 mil
Annular ring (min)	16 mil
Annular ring (%)	25
Annular ring (max)	20 mil
Via drill size	1 mm

Notes about the PCB layout:

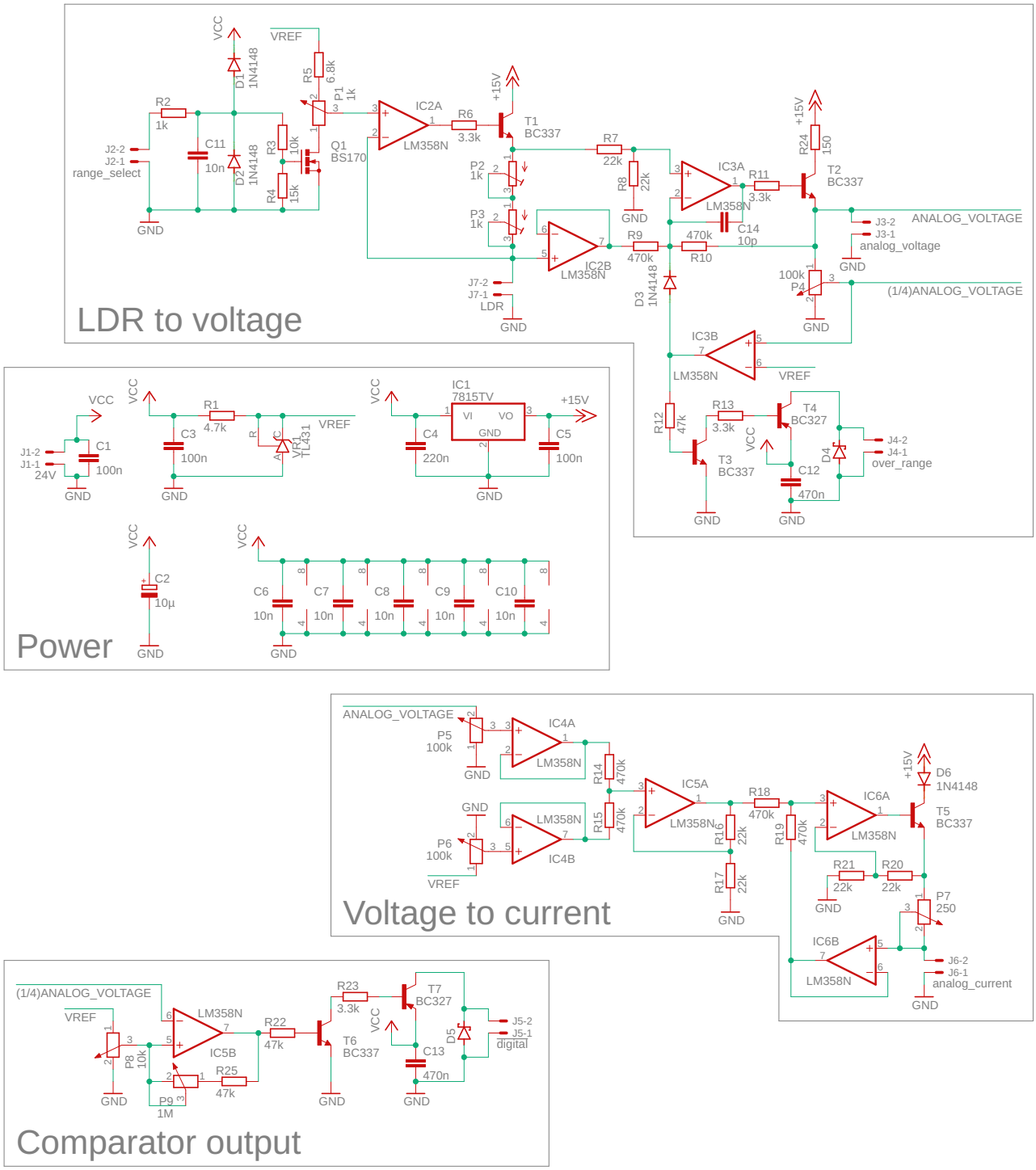
- The top copper layer is only used for a bunch of links and some wires.
- Mounting holes and holes for the heatsink are explained in the previous section.
- Ground plane consists of several manually created polygons to ensure additional clearance near (most) pads. 30 mil isolation could be used instead, but it looks ugly and gets quite close to the pads from every angle.
- Some traces are thicker, usually for signals carrying more current and for power/ground wherever it fits.
- The PNP transistors T4 and T7 are mirrored due to a bug in the components library.
- The 6390B heatsink is partially outside the board area. The better SK104 or SK129 can not be added without moving a lot of components or using less restrictive software.
- *Update:* The holes for the carbon potentiometers turned out to be too tight. The error will not be corrected here.

5.2.1 CAD files

The Eagle schematic and board files are on Gitlab as well as the generated **gerber files**.

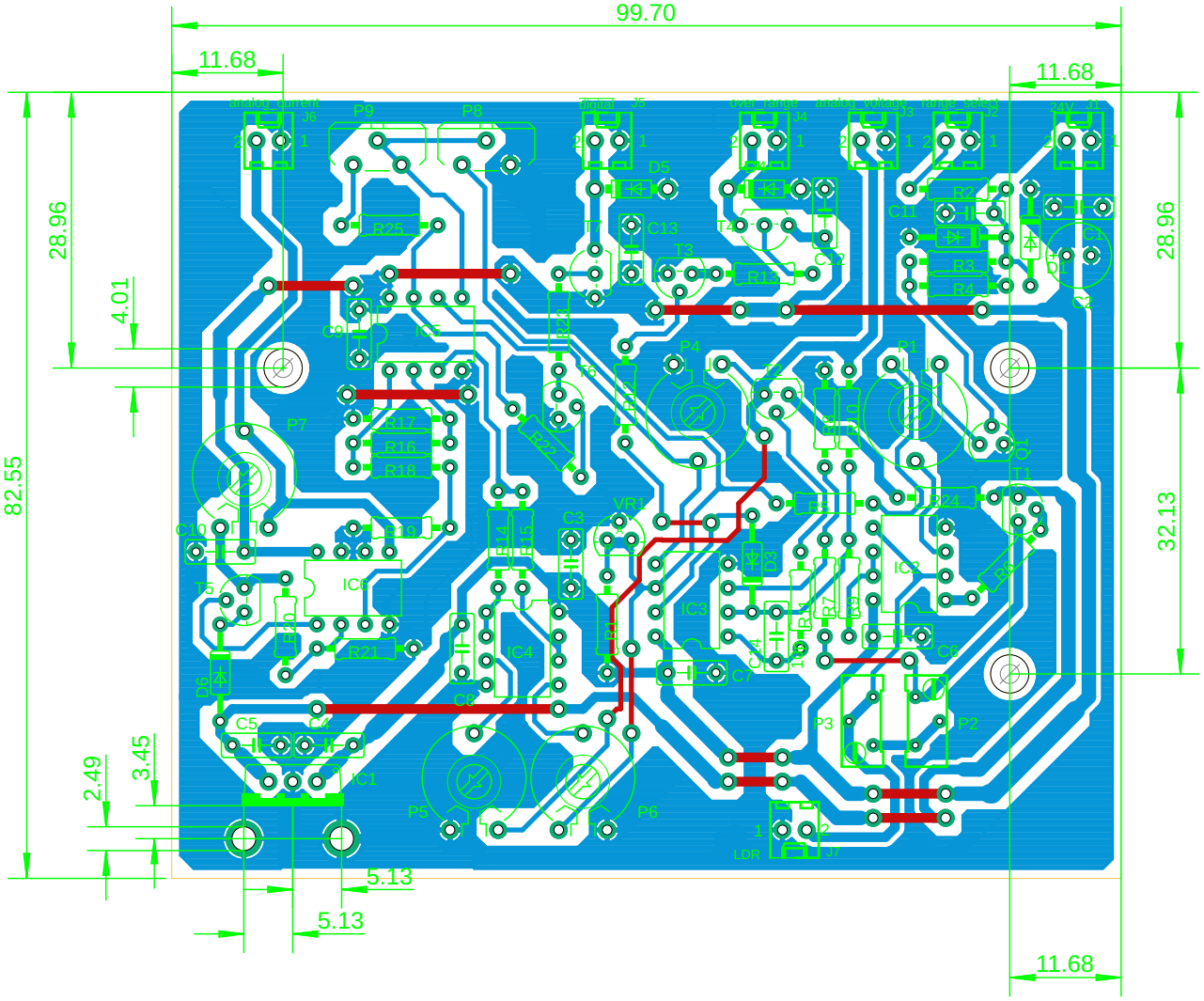
5.2.2 Complete schematic (Eagle)

Update: C14 is supposed to be 100 pF



8/8/20 12:06 AM f=0.78 /home/wine/EAGLE/projects/light-sensor.sch (Sheet: 1/1)

5.2.3 PCB layout (not to scale)



8/17/20 10:28 PM f=1.34 /home/wine/light-sensor-eagle/light-sensor.brd

5.3 Bill of materials

Component designators (*1)	Count	Value / Starelec part#	Eagle footprint	Cost (*2)
C14	1	100 pF ceramic/film	C050-025X075	*
C6 - C11	6	10 nF ceramic/film	C050-025X075	*
C1, C3, C5	3	100 nF ceramic/film	C050-025X075	*
C4	1	220 nF ceramic/film	C050-025X075	*
C12, C13	2	>=220 nF ceramic/film	C050-025X075	*
C2	1	10 μF electrolyic	E2,5-7	*
R24	1	150	0207/10	*
R2	1	1k	0207/10	*
R6, R11, R13, R23	4	3.3k	0207/10	*
R1	1	4.7k	0207/10	*
R5	1	6.8k	0207/10	*
R3	1	10k	0207/10	*
R4	1	15k	0207/10	*
R7-R8, R16-R17, R20-R21	6	22k	0207/10	*
R12, R22, R25	3	47k	0207/10	*
R9-R10, R14-R15, R18-R19	6	470k	0207/10	*
D1-D6	6	1N4148	DO35-10, (*6, *7)	(10) 0.50
P8	1	P10-10K	PT-10S	0.45
P9	1	P10-1M	PT-10S	0.50
P2, P3	2	T910Y-5K	RTRIM64Y	0.80
P7	1	V10-250R	PT-10	0.45
P1	1	V10-1K	PT-10	0.40
P4, P5, P6	3	V10-100K	PT-10	1.20
Q1 (*3)	1	BS170	SOT54E	(5) 1.00
T1-T3, T5-T6 (*3)	5	BC337	TO92	0.50
T4, T7 (*3)	2	BC327	TO92-EBC (*5)	(5) 0.45
VR1	1	TL431CLP	TO92-CLP	0.30
IC1	1	7815CP	TO220V	0.45
IC2 - IC6	5	LM358N	DIL08	2.00
Heatsink	1	6390B	(manual vias)	2.80
Heatsink screw	1	UNC 6-32	(N/A)	
Thermal interface	*	HTC5S (if required)	(N/A)	(1) 2.90
Case	1	1598B	(N/A)	12.80
PCB Screws	3	Self-tapping #6 x 1/4"	(mounting holes)	
LDR	1	PGM5526	(external)	(5) 1.25
J1 - J7 (*4)	7	22-27-2021	22-27-2021-02	(10) 2.40
(*4)	8	22-01-2025	(N/A)	(10) 2.00
(*4)	16	22-01-S	(N/A)	(20) 2.00
Total				35.15

Notes:

1. According to schematic from Eagle. LTspice differs for transistors and ICs.
2. Not including R and C. Sum of the components purchased in minimum quantity, quantities may be specified in parentheses.
3. Transistors can be consolidated. Pretty much any N-MOS, NPN and PNP will do if certain resistor values are checked.
4. Headers and connectors.
5. Eagle footprint is wrong, but component can still be installed.
6. D4 and D5 has a different footprint but will fit at an angle.
7. *Update:* D4 and D5 should preferrably be schottky diodes, but 1N4148 is what has been used

Wires and links (197.5 cm, 0.35 mm^2):

Where	total length	min area	max area	notes
PCB links	10.5 cm		0.75 mm^2	1mm dia hole, use normal links
PCB wires	7.0 cm		0.75 mm^2	1mm dia hole, insulation required
LDR wires	60.0 cm	0.06 mm^2	0.35 mm^2	1x 30 cm pair, 0.35 strongly preferred
I/O and power	120.0 cm	0.06 mm^2	0.35 mm^2	6x 10 cm pairs, 0.35 preferred

Misc:

- PE12-2.5 was removed from the list because the wires are unsuitably thin
- **4x** 4mm washers may or may not be benefical for mounting. Required thickness unknown. The screws are *probably* long enough.

5.4 Assembly

- The row of headers and potentiometers should be placed against the panel of the case.
- There are four screw holes in the case but only three on the board. Soft washers may be required if the leg of R20 pokes too hard into the plastic or if the screw holes are too wide.
- If the case has threaded inserts, the solder joint on the leg of R20 needs to be insulated to prevent a short to ground that would cause U6 to overload itself, P7 and maybe T5.
- Don't screw on the top cover. It will block access to potentiometers during calibration.

Soldering:

- Some links and a few wires are required (red top side traces)
- T4 and T7 are the wrong way on the PCB layout (E and C swapped). Install backwards.
- The giant holes below the 7815 are for the 6390B heatsink, it will extend beyond the PCB.

Resistor divider cherry picking (optional):

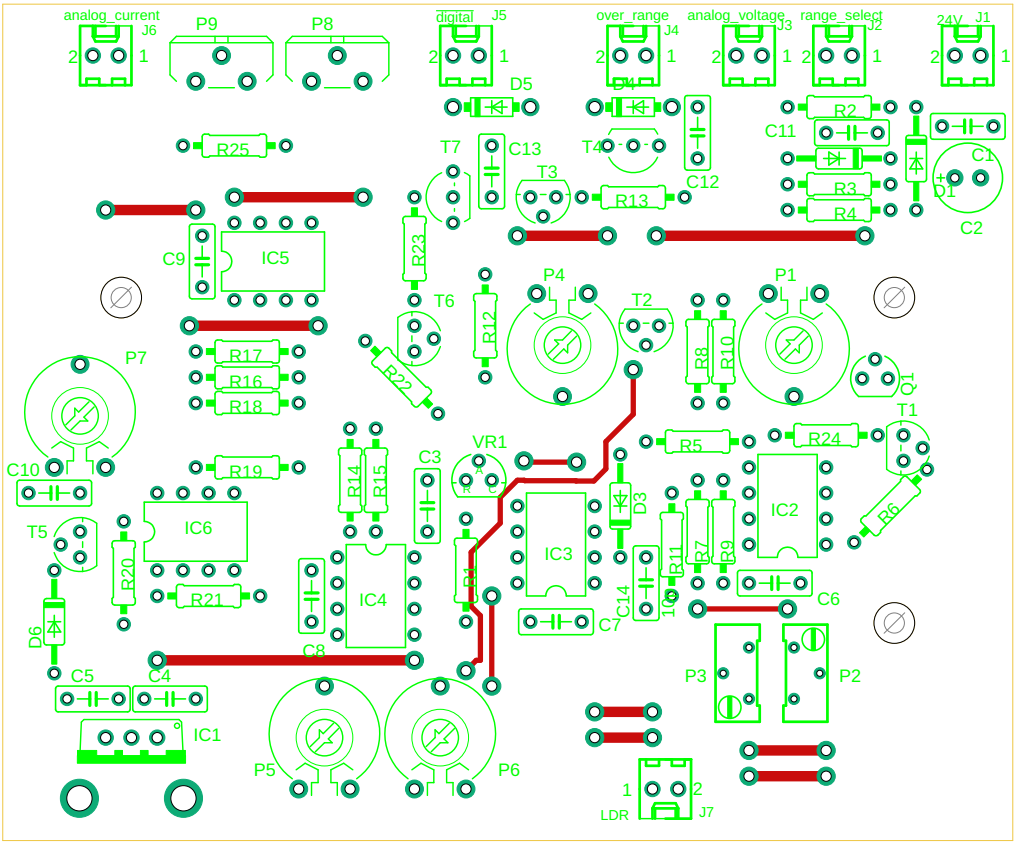
1. Choose R7 (22 kΩ), R8 (22 kΩ), R9 (470 kΩ) and R10 (470 kΩ) to get the smallest possible error from equation 1. This is to get `analog_voltage` as good as possible.
2. Choose R18 (470 kΩ) and R19 (470 kΩ) to get the smallest possible error from equation 2. Choose R20 (22 kΩ) and R21 (22 kΩ) to get the smallest possible error from equation 3.
3. Use the remaining 22 kΩ resistors for R16 and R17. Use the remaining 470 kΩ resistors for R14 and R15.

$$error = \left| \frac{R7 \cdot R10}{R8 \cdot R9} - 1 \right| \tag{1}$$

$$error = \left| \frac{R18}{R19} - 1 \right| \tag{2}$$

$$error = \left| \frac{R20}{R21} - 1 \right| \tag{3}$$

5.4.1 Component locations



5.5 Potentiometer adjustments

5.5.1 After assembly

It is important to set certain trimmers to safe values before applying power.

- P2 plus P3 should be at least 320 Ω together (in series)
- P2 and P3 should be equal
- P5 should be turned no more than 20% from fully counter clockwise
- P6 should be turned no more than 20% from fully clockwise
- P7 should be about 125 Ω

5.5.2 Calibration

These steps assume P2, P3, P5, P6 and P7 are already set to safe values.

`analog_voltage` can be as high as the supply voltage during calibration, do not connect to sensitive equipment.

1. Turn P4 fully clockwise
2. Subject the LDR to 1000 Lux and set `range_select` to low
3. Adjust P2 and P3 equally until `analog_voltage` is 10 V
4. Subject the LDR to 100 000 Lux and set `range_select` to high
5. Adjust P1 until `analog_voltage` is 10 V
6. Keep subjecting the LDR to 100 000 Lux but set `range_select` to low
7. Adjust P4 until `analog_voltage` is 10 V
8. Set P5 fully counter clockwise, P6 fully clockwise and P7 at 50%
9. Adjust P6 until `analog_current` is 4 mA
10. Adjust P5 until `analog_current` is 20 mA

6 Usage/installation instructions

See also the specifications in section 1.2 - Specifications

6.1 Warnings

- Do not apply power before trimmer potentiometers have been set appropriately.
- `range_select` has a rather low upper voltage for logic low. It should be pulled low with low impedance to avoid noise pick up if long wires are used.
- `analog_voltage` has very limited short circuit protection. Prolonged shorts or overloads may cause the smoke to escape from R24.
- `analog_current` has unlimited open circuit protection, but the open circuit voltage may be as high as the supply voltage. Do not connect to sensitive equipment if there is any chance of overload (too much resistance) or breaks.
- `over_range` and $\overline{\texttt{digital}}$ both have no short circuit protection what-so-ever. Any shorts may cause the smoke to leave Q4 respectively Q7 in a spectacular fashion.
- There is not much ESD protection. `range_select` has protection and the digital outputs are probably more tolerant. `analog_current` is likely the most vulnerable.

6.2 Behind the panels

Molex headers and potentiometers behind front panel, from left to right:

Item	Type	Left	Right (/ clockwise)
J1: 24 V	header	shared ground	power in
J2: `range_select`	header	shared ground	digital in
J3: `analog_voltage`	header	shared ground	voltage out
J4: `over_range`	header	return path	digital out
J5: $\overline{\texttt{digital}}$	header	return path	digital out
P8: Threshold level for $\overline{\texttt{digital}}$	potentiometer	0 V	10 V
P9: Hysteresis for $\overline{\texttt{digital}}$	potentiometer	min	max
J6: `analog_current`	header	shared ground	current out

All headers have ground on pin #2 (left pin seen from outside).

The digital outputs do use the same shared ground, but the dedicated return path is much closer to the bypass capacitors for the digital outputs.

The rear side of the board does not extend to the rear panel. The header for the LDR (J7) is on the rear side of the board.

6.3 Transfer functions

`range_select` state	E_{max}
low	1 000 Lux
high	100 000 Lux

$$\texttt{analog\_voltage} = 10\ V \cdot \left(\frac{E}{E_{max}}\right)^{\gamma}$$

$$\texttt{over\_range} = (E > E_{max})$$

$$\overline{\texttt{digital}} = (\texttt{analog\_voltage} < U_{trig})$$

$$\texttt{analog\_current} = 4\ mA + \frac{16\ mA}{10\ V} \cdot \texttt{analog\_voltage}$$

The digital outputs are expressed as boolean values (true = high, false = low), γ is the gamma characteristic of the LDR and E is the illuminance.

U_{trig} is selected by P8 from 0 V to 10 V, but can be quite distorted if P9 is set to a high level of hysteresis.

$$U_{trig,low} = 4 \cdot \frac{\frac{0\ V}{P8 \cdot 10\ k\Omega} + \frac{2.5\ V}{(1-P8) \cdot 10\ k\Omega} + \frac{0\ V}{P9 + 47\ k\Omega}}{\frac{1}{P8 \cdot 10\ k\Omega} + \frac{1}{(1-P8) \cdot 10\ k\Omega} + \frac{1}{P9 + 47\ k\Omega}}$$

$$U_{trig,high} = 4 \cdot \frac{\frac{0\ V}{P8 \cdot 10\ k\Omega} + \frac{2.5\ V}{(1-P8) \cdot 10\ k\Omega} + \frac{U_{out,high}}{P9 + 47\ k\Omega}}{\frac{1}{P8 \cdot 10\ k\Omega} + \frac{1}{(1-P8) \cdot 10\ k\Omega} + \frac{1}{P9 + 47\ k\Omega}}$$

$P8$ is specified as a percentage between 0% and 100% and $P9$ is specified as a resistance between 1 MΩ and 0 Ω.

$U_{out,high}$ is the output voltage of the op-amp which will depend on the supply voltage (19 to 29 V).

See section 3.8 for graphs of the trigger level.

6.4 Plans for testing

The LDR is intended to be wired directly to its connector.

The 6 power and I/O connectors only have bare wires on the other end. Appropriate connections for the ends depend on power supply and test equipment, a large terminal block was previously listen in the bill of materials but has been removed as the wires are far too thin.

The power "cable" *could* have two connectors, one for power (obviously) and one for `range_select`. Connect for high, disconnect for low.

The calibration steps expect a 1000 Lux and 100 000 Lux illumination. If these specific values cannot be produced an alternative would be to replace the LDR with a rheostat (potentiometer) set to a calculated value. This would add yet another connector.

7 BUGS and other known issues

7.1 Potentially power hungry

This circuit may waste a lot of power (in pessimal conditions).

The 7815 needs a heatsink because it supplies up to 87 mA at a voltage drop that can be as high as $29\ V - 14.25\ V = 14.75\ V$ and up to 8 mA quiescent current.
The 15 V rail exists to save three transistors from the very same fate. Max power dissipation is 1.52 W.

Depending on the resistance of the LDR the current through it and Q1 could be as high as 47 mA (which would be pretty bad). The analog voltage output can supply up to 20 mA, and the analog current output goes up to 20 mA.

Power dissipation in the LDR might slightly exceed the 100 mW limit in the worst case:

$$P = 2.5\ V \cdot \frac{(15.75\ V - 2.5\ V - 0.2\ V)}{320\ \Omega} = 102\ mW$$

It also need two large cermet trimmer potentiometers to dissipate up to 0.7 Watts.

A much better approach would be to use a lower voltage on the LDR and lower resistance in the potentiometer and have gain > 1 in the differential amplifier.

7.2 Problems with $\overline{\texttt{digital}}$

The digital output compares the analog output voltage against a "fixed" value. It does not know if the device is in the 1000 lux scale or in the 100 000 lux scale.

The variable hysteresis is not well designed; it's very asymetric and depends heavily on the trigger level.

The name is also stupid and the not bar adds a layer of confusion. It should be renamed to `dark` which is completely unambiguous.

P9 could be larger (2M to 10M) and logarithmic, R25 could be twice as large. There is an insane amount of hysteresis.

7.3 Lazy design of the U-to-I convertee

U7 and U8 could be removed if some effort was spent on calculating a resistor network. U9 could also be removed by adjusting the gain at P7.

P7 is also useless and could be replaced with a fixed resistor. P5 and P6 offer enough calibration opportunities.

7.4 Simulation limitations

The UniversalOpamp2 op-amp has been used instead of a (somewhat) accurate model of the LM358.

7.5 `range_select` logic low voltage

The actual maximum low voltage is unknown. The voltage divider conducts 320 μA, while it is more than the maximum cut-off current (0.5 μA) it's also less than the threshold current (1 mA).

The input should be redesigned to properly drive the MOSFET. But that would require actual work.

It does seem to work well enough in the simulation though.

Workarounds:

- Pull to ground with low impedance (CMOS, NMOS, mechanical switch)
- Saturated NPN (0.3 V) and hope for the best
- A 470 Ω (*1) to 3.3 kΩ (*2) bodge resistor can be added in parallel with R5 and P1.

$$2.5\ V / \frac{10\ mV}{R_{DS(on),typ} = 1.8\ \Omega} = 450\ \Omega \tag{1}$$

$$2.5\ V / (1\ mA - \frac{2.5\ V}{7.8\ k\Omega}) = 3679\ \Omega \tag{2}$$

7.6 Should C14 be placed between Q2 base and ground instead?

Doing this change would require simulating all those things again, and it seems to work well enough as it is.

If there was any time, it should probably be investigated if moving C14 like this would have any advantages.

But it should also be noted that this has only yet been seen in a simulation, the only thing what matters is what the actual circuit does.

EMC wasn't supposed to be a problem, but apparently it might still be.

8 Errata

This first part has been updated on the 9th and 21st of December 2020.

- C14 has always been intended to be 100 pF but all schematics show 10 pF
- D4 and D5 should probably be schottky diodes if anyone is insane enough to actually build this circuit
- Some issues with the PCB design have been noted but not corrected
- The partial schematics show C12 and C13 as 100 nF, that's wrong.
- A few minor corrections and clarifications that are not noteworthy.